

# SYNCHRONOUS DRAM

1X16Y3VTW - 512K x 16 x 2 banks

## FEATURES

- PC100 functionality
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- 1 Meg x 16 - 512K x 16 x 2 banks architecture with 11 row, 8 column addresses per bank
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge Mode, includes CONCURRENT AUTO PRECHARGE
- Self Refresh and Adaptable Auto Refresh Modes
  - 32ms, 2,048-cycle refresh or
  - 64ms, 2,048-cycle refresh or
  - 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply
- Supports CAS latency of 1, 2 and 3
- Industrial temperature range: -40°C to +85°C

## OPTIONS

- Configuration
  - 1 Meg x 16 (512K x 16 x 2 banks)
- Device Technology
  - SDR SDRAM/ 3.3 Vdd
- Plastic Package - OCPL\*
  - 50-pin TSOP (400 mil)
- Timing (Cycle Time)
  - 6ns (166 MHz)
  - 7ns (143 MHz)
  - 8ns (125 MHz)
- Operating Temperature
  - 40°C to +85°C

## MARKING

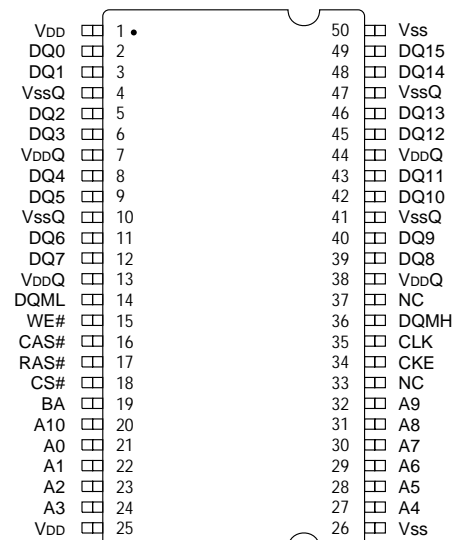
- 1X16
- Y3V
- TW
- 6
- 7
- 8E
- I

## KEY TIMING PARAMETERS

SPEED	CLOCK	ACCESS TIME CL = 3**	SETUP	HOLD
-6	166 MHz	5.5ns	2ns	1ns
-7	143 MHz	5.5ns	2ns	1ns
-8E	+125 MHz	6ns	2ns	1ns

\*Off-center parting line  
\*\*CL = CAS (READ) latency

## PIN ASSIGNMENT (Top View) 50-Pin TSOP



Note: The # symbol indicates signal is active LOW.

	1 Meg x 16
Configuration	512K x 16 x 2 banks
Refresh Count	2K or 4K
Row Addressing	2K (A0-A10)
Bank Addressing	2 (BA)
Column Addressing	256 (A0-A7)

## 16Mb (x16) SDRAM PART NUMBER

PART NUMBER	ARCHITECTURE
1X16Y3VTW	1 Meg x 16

## GENERAL DESCRIPTION

The 16Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 16,777,216 bits. It is internally configured as a dual 512K x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 512K x 16-bit banks is organized as 2,048 rows by 256 columns by 16 bits. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed

## GENERAL DESCRIPTION (continued)

sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA selects the bank, A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 1 Meg x 16 SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2/7rule of prefetch architectures,

but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The 1 Meg x 16 SDRAM is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

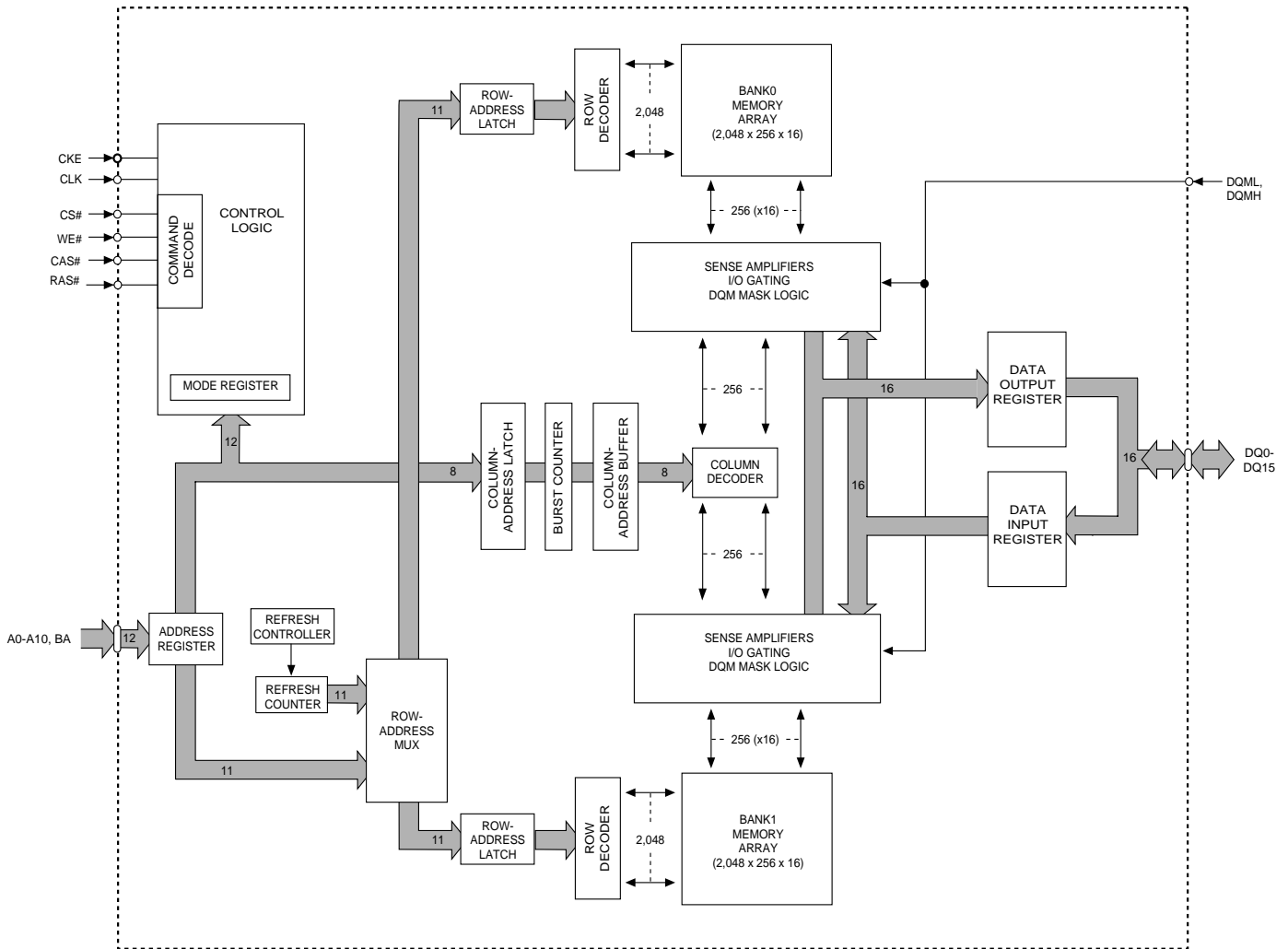
## TABLE OF CONTENTS (for full data sheet)

Functional Block Diagram - 1 Meg x 16 .....	3
Pin Descriptions .....	4
<b>Functional Description</b> .....	5
Initialization .....	5
Register Definitions .....	5
Mode Register .....	5
Burst Length .....	5
Burst Type .....	5
CAS Latency .....	7
Operating Mode .....	7
Write Burst Mode .....	7
<b>Commands</b> .....	8
<i>Truth Table 1 (Commands and DQM Operation)</i> .....	8
Command Inhibit .....	9
No Operation (NOP) .....	9
Load Mode Register .....	9
Active .....	9
Read .....	9
Write .....	9
Precharge .....	9
Auto Precharge .....	9
Burst Terminate .....	9
Auto Refresh .....	10
Self Refresh .....	10
Absolute Maximum Ratings .....	11
DC Electrical Characteristics and Operating Conditions ....	11
IDD Specifications and Conditions .....	11
Capacitance .....	12
<b>AC Electrical Characteristics (Timing Table)</b> .....	12

## Timing Waveforms

Initialize and Load Mode Register .....	15
Power-Down Mode .....	16
Clock Suspend Mode .....	17
Auto Refresh Mode .....	18
Self Refresh Mode .....	19
Reads	
Read - Single Read .....	20
Read - Without Auto Precharge .....	21
Read - With Auto Precharge .....	22
Alternating Bank Read Accesses .....	23
Read - Full-Page Burst .....	24
Read - DQM Operation .....	25
Writes	
Write - Single Write .....	26
Write - Without Auto Precharge .....	27
Write - With Auto Precharge .....	28
Alternating Bank Write Accesses .....	29
Write - Full-Page Burst .....	30
Write - DQM Operation .....	31

**FUNCTIONAL BLOCK DIAGRAM**  
**1 Meg x 16 SDRAM**



## PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
35	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
34	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), ACTIVE POWER-DOWN (row ACTIVE in either bank) or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
18	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
15, 16, 17	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
14, 36	DQML, DQMH	Input	Input/Output Mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. DQML corresponds to DQ0-DQ7; DQMH corresponds to DQ8-DQ15. DQML and DQMH are considered same state when referenced as DQM.
19	BA	Input	Bank Address Inputs: BA defines to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA is also used to program the twelfth bit of the Mode Register.
21-24, 27-32, 20	A0-A10	Input	Address Inputs: A0-A10 are sampled during the ACTIVE command (row-address A0-A10) and READ/WRITE command (column-address A0-A7, with A10 defining AUTO PRECHARGE) to select one location out of the 512K available in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2, 3, 5, 6, 8, 9, 11, 12, 39, 40, 42, 43, 45, 46, 48, 49	DQ0-DQ15	Input/Output	Data I/Os: Data bus.
33, 37	NC	--	No Connect: These pins should be left unconnected.
7, 13, 38, 44	V <sub>DDQ</sub>	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
4, 10, 41, 47	V <sub>SSQ</sub>	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
1, 25	V <sub>DD</sub>	Supply	Power Supply: +3.3V ±0.3V.
26, 50	V <sub>SS</sub>	Supply	Ground.

## FUNCTIONAL DESCRIPTION

In general, the SDRAM is a dual 512K x 16 DRAM that operates at 3.3V and includes a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 512K x 16-bit banks is organized as 2,048 rows by 256 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA selects the bank, A0-A10 select the row). The address bits (A0-A7) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

### Initialization

SDRAMs must be powered up and initialized in a pre-defined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to V<sub>DD</sub> and V<sub>DDQ</sub> (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100μs delay prior to applying any command other than a COMMAND INHIBIT or a NOP. Starting at some point during this 100μs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100μs delay has been satisfied, with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for Mode Register programming. Because the Mode Register will power up in an unknown state, it should be loaded prior to applying any operational command.

## Register Definition

### MODE REGISTER

The Mode Register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in Figure 1. The Mode Register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode Register bits M0-M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4-M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 and M11 are reserved for future use.

The Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

### Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 1. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4 or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

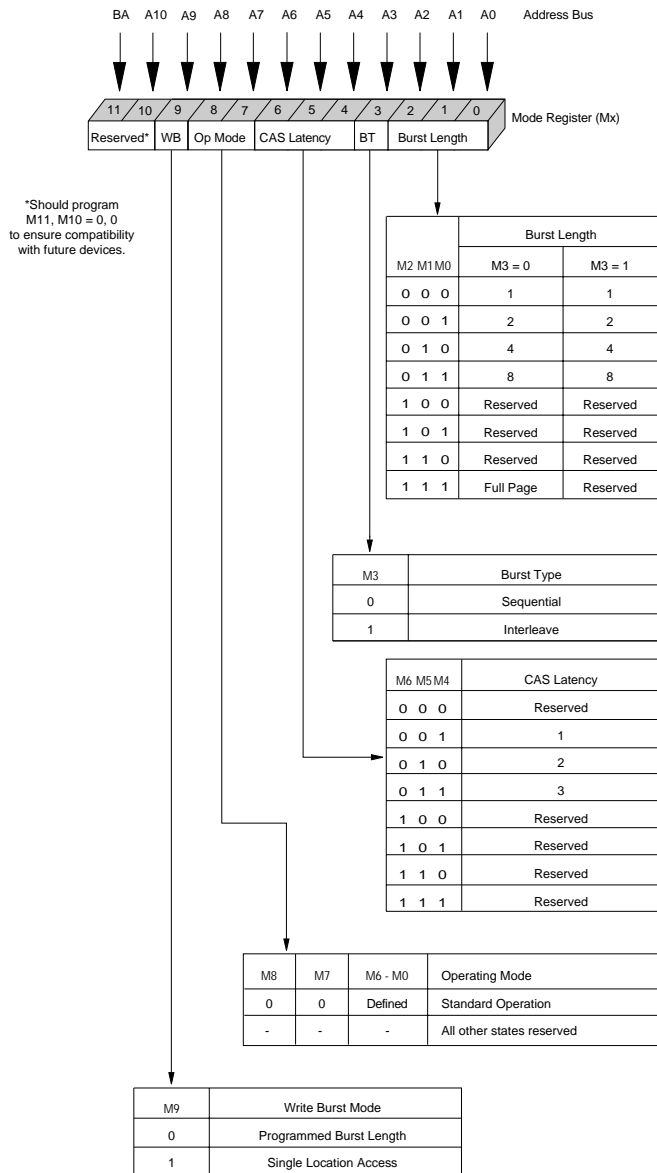
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A7 when the burst length is set to two, by A2-A7 when the burst length is set to four and by A3-A7 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

### Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 1.



**Figure 1**  
**MODE REGISTER DEFINITION**

**Table 1**  
**BURST DEFINITION**

Burst Length	Starting Column Address	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	
Full Page (256)	n = A0-A7 (location 0-255)	Cn, Cn+1, Cn+2 Cn+3, Cn+4... Cn-1, Cn	Not supported

- NOTE:**
- For a burst length of two, A1-A7 select the block of two burst; A0 selects the starting column within the block.
  - For a burst length of four, A2-A7 select the block of four burst; A0-A1 select the starting column within the block.
  - For a burst length of eight, A3-A7 select the block of eight burst; A0-A2 select the starting column within the block.
  - For a full-page burst, the full row is selected and A0-A7 select the starting column.
  - Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
  - For a burst length of one, A0-A7 select the unique column to be accessed, and Mode Register bit M3 is ignored.

## CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to 1, 2 or 3 clocks.

If a READ command is registered at clock edge  $n$ , and the latency is  $m$  clocks, the data will be available by clock edge  $n + m$ . The DQs will start driving as a result of the clock edge one cycle earlier ( $n + m - 1$ ), and provided that the relevant access times are met, the data will be valid by clock edge  $n + m$ . For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at  $T_0$ , and the latency is programmed to two clocks, the DQs will start driving after  $T_1$  and the

data will be valid by  $T_2$ , as shown in Figure 2. Table 2 below indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

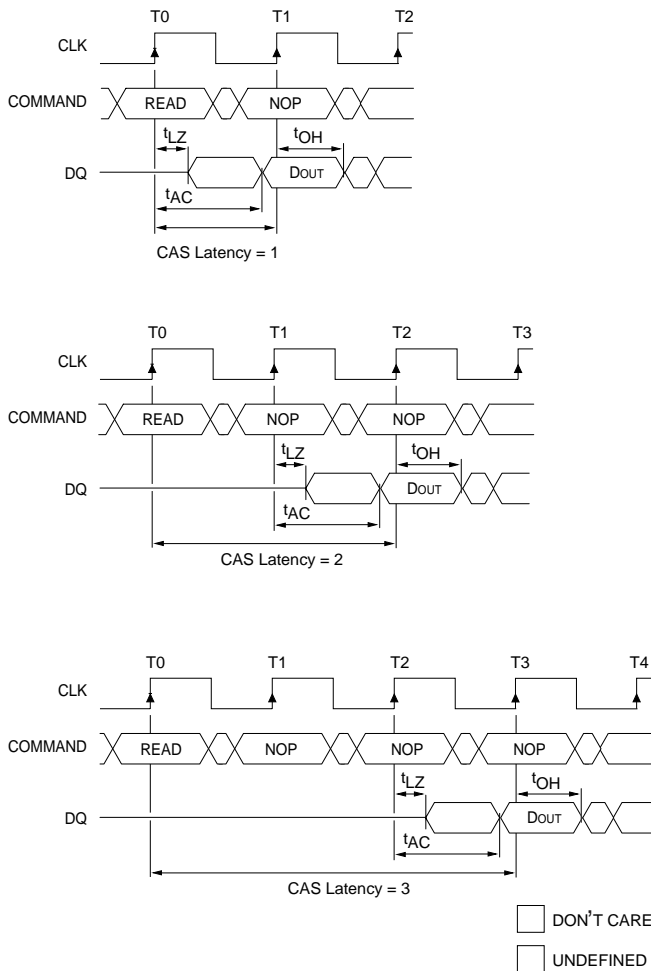
## Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

## Write Burst Mode

When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.



**Figure 2**  
**CAS LATENCY**

**Table 2**  
**CAS LATENCY**

SPEED	ALLOWABLE OPERATING FREQUENCY (MHz)		
	CAS LATENCY = 1	CAS LATENCY = 2	CAS LATENCY = 3
-7	≤ 50	≤ 125	≤ 166
-75	≤ 40	≤ 100	≤ 143
-8E	≤ 40	≤ 77	≤ 125

## COMMANDS

Truth Table 1 provides a quick reference of available commands. This is followed by a written description of each command. Three additional Truth Tables appear following

the Operation section; these tables provide current state/next state information.

## TRUTH TABLE 1 -- Commands and DQM Operation

(Notes: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column and start READ burst)	L	H	L	H	L/H <sup>8</sup>	Bank/Col	X	4
WRITE (Select bank and column and start WRITE burst)	L	H	L	L	L/H <sup>8</sup>	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	2
Write Enable/Output Enable	-	-	-	-	-	-	Active	8
Write Inhibit/Output High-Z	-	-	-	-	H	-	High-Z	8

- NOTE:**
1. CKE is HIGH for all commands shown except SELF REFRESH.
  2. A0-A10 and BA define the op-code written to the Mode Register.
  3. A0-A10 provide row address, and BA determines which bank is made active.
  4. A0-A7 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA determines which bank is being read from or written to.
  5. For A10 LOW, BA determines which bank is being precharged; for A10 HIGH, all banks are precharged and BA is a "Don't Care".
  6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
  7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
  8. Activates or deactivates the DQs during WRITES (zero-clock delay) and READS (two-clock delay).

### COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

### NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM which is selected (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

### LOAD MODE REGISTER

The Mode Register is loaded via inputs A0-A10 and BA. See Mode Register heading in Register Definition section. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until <sup>t</sup>MRD is met.

### ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA input selects the bank, and the address provided on inputs A0-A10 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

### READ

The READ command is used to initiate a burst read access to an active row. The value on the BA input selects the bank, and the address provided on inputs A0-A7 selects the starting column location. The value on input A10 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of the READ burst; if AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses. Read data appears on the DQs, subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQs will be High-Z two clocks later; if the DQM signal was registered LOW, the DQs will provide valid data.

### WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA input selects the bank, and the address provided on inputs A0-A7 selects the starting column location. The value on input A10 determines whether or not AUTO PRECHARGE is used. If

AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of the WRITE burst; if AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

### PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (<sup>t</sup>RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, input BA selects the bank. Otherwise BA is treated as "Don't Care". Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

### AUTO PRECHARGE

AUTO PRECHARGE is a feature which performs the same individual-bank PRECHARGE function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst, except in the full-page burst mode, where AUTO PRECHARGE does not apply. AUTO PRECHARGE is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command.

AUTO PRECHARGE ensures that the PRECHARGE is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (<sup>t</sup>RP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

### BURST TERMINATE

The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated as shown in the Operation section of this data sheet.

**AUTO REFRESH**

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) REFRESH in conventional DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required.

The addressing during an AUTO REFRESH command is generated by an internal refresh controller. This means that the address lines are not used to generate the refresh address and are "Don't Care".

The 1 Meg x 16 SDRAM requires 2,048 AUTO REFRESH cycles every 64ms (<sup>t</sup>REF) to ensure that each row is refreshed. Distributed refresh can be achieved by providing an AUTO REFRESH command once every 31.25 $\mu$ s. Burst refresh can be accomplished by issuing 2,048 AUTO REFRESH commands consecutively at the minimum cycle rate of <sup>t</sup>RC.

To provide a 4K refresh scheme, the refresh rate would be doubled. Thus, 2,048 AUTO-REFRESH commands distributed every 15.625 $\mu$ s would allow the 1 Meg x 16 SDRAM to have a 4K refresh if required. Of the three types of refresh options, utilizing the 2,048 cycles every 64ms (31.25 $\mu$ s per refresh) provides the maximum power savings.

**SELF REFRESH**

The SELF REFRESH command can be used to retain data in the SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SDRAM become "Don't Care", with the exception of CKE, which must remain LOW.

Once self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own auto refresh cycles. The SDRAM must remain in self refresh mode for a minimum period equal to <sup>t</sup>RAS, and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) prior to CKE going back HIGH. Once CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for <sup>t</sup>XSR, because time is required for the completion of any internal refresh in progress.

Upon exiting self refresh mode, AUTO REFRESH commands may be issued every 15.625 $\mu$ s or less as both SELF REFRESH and AUTO REFRESH utilize the row refresh counter.

## ABSOLUTE MAXIMUM RATINGS\*

Voltage on V <sub>DD</sub> , V <sub>DDQ</sub> Supply	
Relative to V <sub>SS</sub> .....	-1V to +4.6V
Voltage on Inputs, NC or I/O Pins	
Relative to V <sub>SS</sub> .....	-1V to +4.6V
Operating Temperature, T <sub>A</sub> (ambient) .....	-40°C to +85°C
Storage Temperature (plastic) .....	-55°C to +150°C
Power Dissipation .....	1W

\*Stresses greater than those listed under Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 6) (-40°C ≤ T<sub>A</sub> ≤ +85°C; V<sub>DD</sub>, V<sub>DDQ</sub> = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V <sub>DD</sub> , V <sub>DDQ</sub>	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V <sub>IH</sub>	2.2	V <sub>DD</sub> + 0.3	V	22
INPUT LOW VOLTAGE: Logic 0; All inputs	V <sub>IL</sub>	-0.3	0.8	V	22
INPUT LEAKAGE CURRENT: Any input 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> (All other pins not under test = 0V)	I <sub>I</sub>	-5	5	μA	
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V <sub>OUT</sub> ≤ V <sub>DDQ</sub>	I <sub>OZ</sub>	-10	10	μA	
OUTPUT LEVELS: Output High Voltage (I <sub>OUT</sub> = -4mA)	V <sub>OH</sub>	2.4	--	V	
Output Low Voltage (I <sub>OUT</sub> = 4mA)	V <sub>OL</sub>	--	0.4	V	

## I<sub>DD</sub> SPECIFICATIONS AND CONDITIONS

(Notes: 1, 6, 11, 13) (-40°C ≤ T<sub>A</sub> ≤ +85°C; V<sub>DD</sub>, V<sub>DDQ</sub> = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-7	-75	-8E		
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; t <sub>RC</sub> = t <sub>RC</sub> (MIN); CAS latency = 3	I <sub>DD1</sub>	145	140	135	mA	3, 18, 19, 26
STANDBY CURRENT: Power-Down Mode; CKE = LOW; All banks idle	I <sub>DD2</sub>	2	2	2	mA	26
STANDBY CURRENT: Active Mode; CS# = HIGH; CKE = HIGH; All banks active after t <sub>RCD</sub> met; No accesses in progress	I <sub>DD3</sub>	45	40	35	mA	3, 12, 19, 26
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active, CAS latency = 3	I <sub>DD4</sub>	140	130	100	mA	3, 18, 19, 26
AUTO REFRESH CURRENT: t <sub>RC</sub> = 15.625μs; CAS latency = 3; CS# = HIGH; CKE = HIGH	I <sub>DD5</sub>	45	40	35	mA	3, 12, 18, 19, 26
SELF REFRESH CURRENT: CKE ≤ 0.2V	I <sub>DD6</sub>	1	1	1	mA	4

## CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CLK	C <sub>I1</sub>	2.5	4.0	pF	2
Input Capacitance: All other input-only pins	C <sub>I2</sub>	2.5	5.0	pF	2
Input/Output Capacitance: DQs	C <sub>IO</sub>	4.0	6.5	pF	2

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 8, 9, 11) (-40°C ≤ T<sub>A</sub> ≤ +85°C)

AC CHARACTERISTICS			-7		-75		-8E			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from CLK (pos. edge)	CL = 3	t <sup>AC</sup>		5.5		5.5		6	ns	
	CL = 2	t <sup>AC</sup>		8		8.5		9	ns	22
	CL = 1	t <sup>AC</sup>		18		22		22	ns	22
Address hold time		t <sup>AH</sup>	1		1		1		ns	
Address setup time		t <sup>AS</sup>	2		2		2		ns	
CLK high level width		t <sup>CH</sup>	2.5		2.75		3		ns	
CLK low level width		t <sup>CL</sup>	2.5		2.75		3		ns	
Clock cycle time	CL = 3	t <sup>CK</sup>	6		7		8		ns	23
	CL = 2	t <sup>CK</sup>	8		10		13		ns	22, 23
	CL = 1	t <sup>CK</sup>	20		25		25		ns	23
CKE hold time		t <sup>CKH</sup>	1		1		1		ns	
CKE setup time		t <sup>CKS</sup>	2		2		2		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		t <sup>CMH</sup>	1		1		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		t <sup>CMS</sup>	2		2		2		ns	
Data-in hold time		t <sup>DH</sup>	1		1		1		ns	
Data-in setup time		t <sup>DS</sup>	2		2		2		ns	
Data-out high-impedance time	CL = 3	t <sup>HZ</sup>		5.5		5.5		6	ns	10
	CL = 2	t <sup>HZ</sup>		6		8.5		9	ns	10
	CL = 1	t <sup>HZ</sup>		18		22		22	ns	10
Data-out low-impedance time		t <sup>LZ</sup>	1		1		1		ns	
Data-out hold time		t <sup>OH</sup>	1.5		1.5		1.5		ns	
ACTIVE to PRECHARGE command		t <sup>RAS</sup>	42	120,000	42	120,000	48	120,000	ns	
AUTO REFRESH, ACTIVE command period		t <sup>RC</sup>	60		70		80		ns	22
AUTO REFRESH period		t <sup>RCAR</sup>	66		70		80		ns	
ACTIVE to READ or WRITE delay		t <sup>RCD</sup>	18		20		24		ns	22
Refresh period - 2,048 or 4,096 rows		t <sup>REF</sup>		64		64		64	ms	
PRECHARGE command period		t <sup>RP</sup>	18		21		24		ns	22
ACTIVE bank A to ACTIVE bank B command		t <sup>RRD</sup>	12		14		16		ns	
Transition time		t <sup>T</sup>	0.3	1.2	0.3	1.2	0.3	10	ns	7
WRITE recovery time		t <sup>WR</sup>	1 + 4ns		1 + 3ns		1 + 2ns		t <sup>CK</sup>	24
			10		10		10		ns	25
Exit SELF REFRESH to ACTIVE command		t <sup>XSR</sup>	80		80		80		ns	20

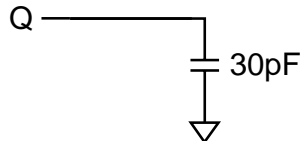
**AC FUNCTIONAL CHARACTERISTICS**

 (Notes: 5, 6, 7, 8, 9, 11) ( $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ )

PARAMETER	SYMBOL	-7	-75	-8E	UNITS	NOTES	
READ/WRITE command to READ/WRITE command	$t^{\text{CCD}}$	1	1	1	$t^{\text{CK}}$	17	
CKE to clock disable or power-down entry mode	$t^{\text{CKED}}$	1	1	1	$t^{\text{CK}}$	14	
CKE to clock enable or power-down exit setup mode	$t^{\text{PED}}$	1	1	1	$t^{\text{CK}}$	14	
DQM to input data delay	$t^{\text{DQD}}$	0	0	0	$t^{\text{CK}}$	17	
DQM to data mask during WRITES	$t^{\text{DQM}}$	0	0	0	$t^{\text{CK}}$	17	
DQM to data high-impedance during READs	$t^{\text{DQZ}}$	2	2	2	$t^{\text{CK}}$	17	
WRITE command to input data delay	$t^{\text{DWD}}$	0	0	0	$t^{\text{CK}}$	17	
Data-in to ACTIVE command	CL = 3	$t^{\text{DAL}}$	5	5	5	$t^{\text{CK}}$	15, 21
	CL = 2	$t^{\text{DAL}}$	4	4	4	$t^{\text{CK}}$	15, 21
	CL = 1	$t^{\text{DAL}}$	3	3	3	$t^{\text{CK}}$	15, 21
Data-in to PRECHARGE	$t^{\text{DPL}}$	2	2	2	$t^{\text{CK}}$	16	
Last data-in to burst STOP command	$t^{\text{BDL}}$	0	0	0	$t^{\text{CK}}$	17	
Last data-in to new READ/WRITE command	$t^{\text{CDL}}$	1	1	1	$t^{\text{CK}}$	17	
Last data-in to PRECHARGE command	$t^{\text{RDL}}$	1	1	1	$t^{\text{CK}}$	16, 21	
LOAD MODE REGISTER command to ACTIVE or REFRESH command	$t^{\text{MRD}}$	2	2	2	$t^{\text{CK}}$	26	
Data-out to high-impedance from PRECHARGE command	CL = 3	$t^{\text{ROH}}$	3	3	3	$t^{\text{CK}}$	17
	CL = 2	$t^{\text{ROH}}$	2	2	2	$t^{\text{CK}}$	17
	CL = 1	$t^{\text{ROH}}$	1	1	1	$t^{\text{CK}}$	17

## NOTES

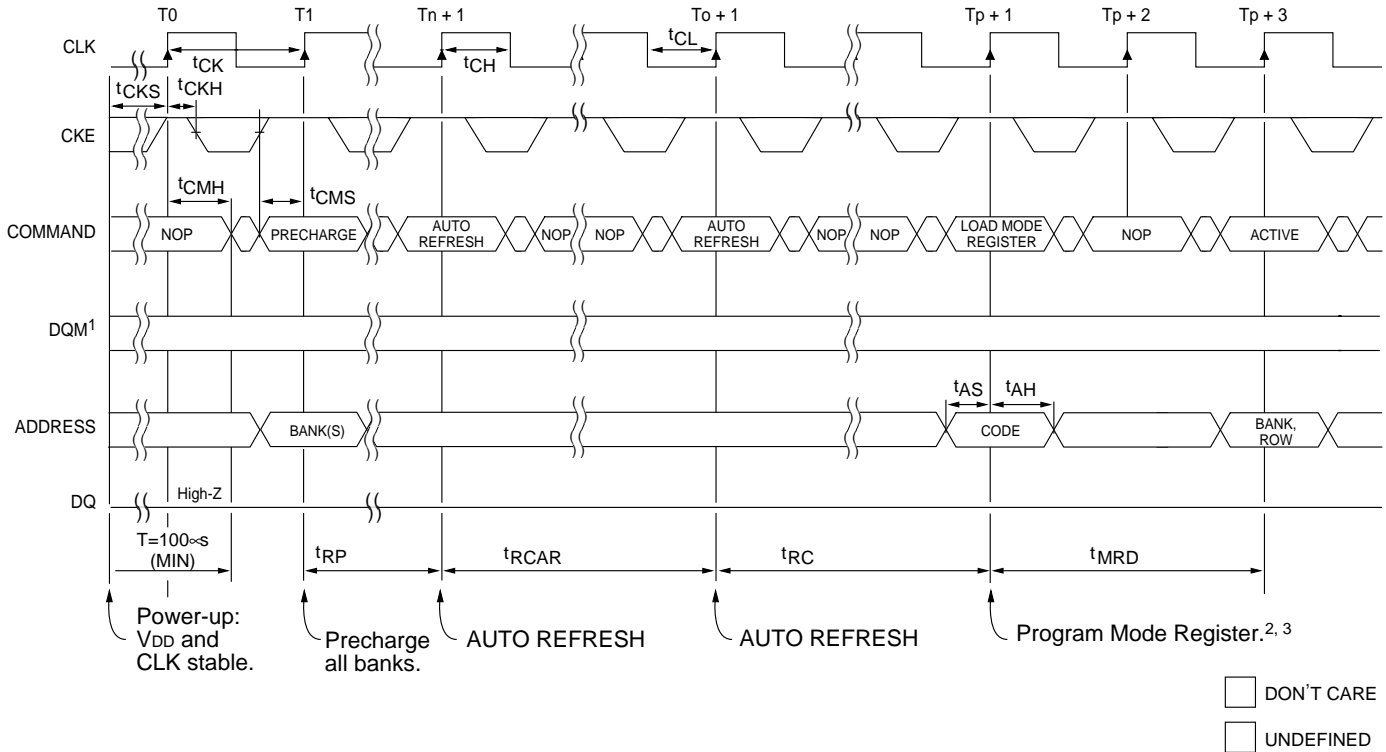
1. All voltages referenced to  $V_{SS}$ .
2. This parameter is sampled.  $V_{DD}$ ,  $V_{DDQ} = +3.3V$ ;  $f = 1\text{ MHz}$ ,  $T_A = 25^\circ\text{C}$ .
3.  $I_{DD}$  is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ( $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ ) is ensured.
6. An initial pause of  $100\mu\text{s}$  is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. ( $V_{DD}$  and  $V_{DDQ}$  must be powered up simultaneously.  $V_{SS}$  and  $V_{SSQ}$  must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the  $t_{REF}$  refresh requirement is exceeded.
7. AC characteristics assume  $t_T = 1\text{ ns}$ .
8. In addition to meeting the transition rate specification, the clock and CKE must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
9. Outputs measured at  $1.5V$  with equivalent load:



10.  $t_{HZ}$  defines the time at which the output achieves the open circuit condition; it is not a reference to  $V_{OH}$  or  $V_{OL}$ . The last valid data element will meet  $t_{OH}$  before going High-Z.
11. AC timing and  $I_{DD}$  tests have  $V_{IL} = 0V$  and  $V_{IH} = 3V$  with timing referenced to  $1.5V$  crossover point.

12. Other input signals are allowed to transition no more than once in any two-clock period and are otherwise at valid  $V_{IH}$  or  $V_{IL}$  levels.
13.  $I_{DD}$  specifications are tested after the device is properly initialized.
14. Timing actually specified by  $t_{CKS}$ ; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by  $t_{WR}$  plus  $t_{RP}$ ; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by  $t_{WR}$ .
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The  $I_{DD}$  current will decrease as the CAS latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS latency is reduced.
19. Address transitions average one transition every two-clock period.
20. CLK must be toggled a minimum of two times during this period.
21. Based on  $t_{CK} = 166\text{ MHz}$  for -7,  $143\text{ MHz}$  for -75 and  $125\text{ MHz}$  for -8E.
22.  $V_{IH}$  overshoot:  $V_{IH}(\text{MAX}) = V_{DDQ} + 2V$  for a pulse width  $\leq 3\text{ ns}$ , and the pulse width cannot be greater than one third of the cycle rate.  $V_{IL}$  undershoot:  $V_{IL}(\text{MIN}) = -2V$  for a pulse width  $\leq 3\text{ ns}$ . The pulse width cannot be greater than one third of the cycle rate.
23. The clock frequency must remain constant during access or precharge states (READ, WRITE, including  $t_{WR}$ , and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only.
25. Precharge mode only.
26.  $t_{CK} = 6\text{ ns}$  for -7,  $7\text{ ns}$  for -75,  $8\text{ ns}$  for -8E.

## INITIALIZE AND LOAD MODE REGISTER



## TIMING PARAMETERS

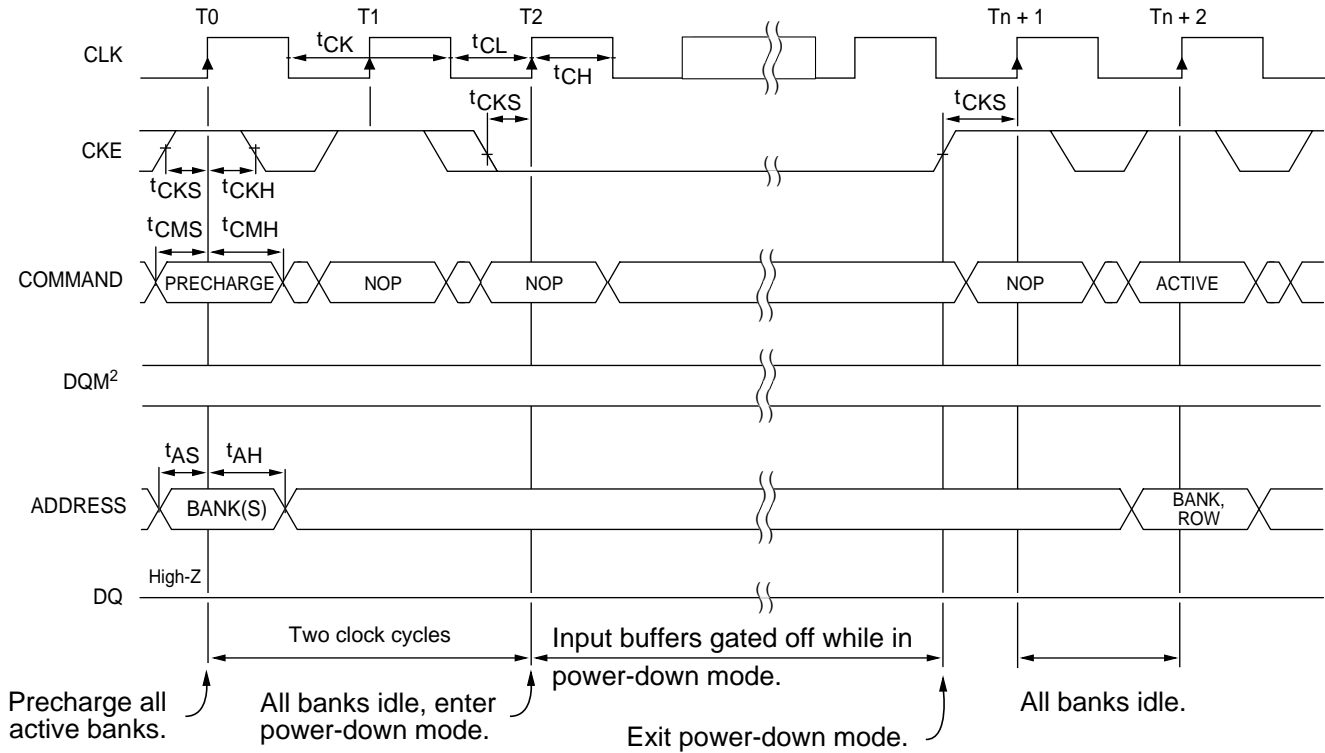
SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>AH</sub>	1		1		1		ns
t <sub>AS</sub>	2		2		2		ns
t <sub>CH</sub>	2.5		2.75		3		ns
t <sub>CL</sub>	2.5		2.75		3		ns
t <sub>CK</sub> (3)	6		7		8		ns
t <sub>CK</sub> (2)	8		10		13		ns
t <sub>CK</sub> (1)	20		25		25		ns
t <sub>CKH</sub>	1		1		1		ns

SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>CKS</sub>	2		2		2		ns
t <sub>CMH</sub>	1		1		1		ns
t <sub>CMS</sub>	2		2		2		ns
t <sub>MRD</sub>	2		2		2		t <sub>CK</sub>
t <sub>RC</sub>	60		70		80		ns
t <sub>RCAR</sub>	66		70		80		ns
t <sub>RP</sub>	18		21		24		ns

\*CAS latency indicated in parentheses.

- NOTE:**
1. DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.
  2. The Mode Register may be loaded prior to the AUTO REFRESH cycles if desired.
  3. Outputs are guaranteed High-Z after command is issued.

## POWER-DOWN MODE <sup>1</sup>



□ DON'T CARE  
 □ UNDEFINED

## TIMING PARAMETERS

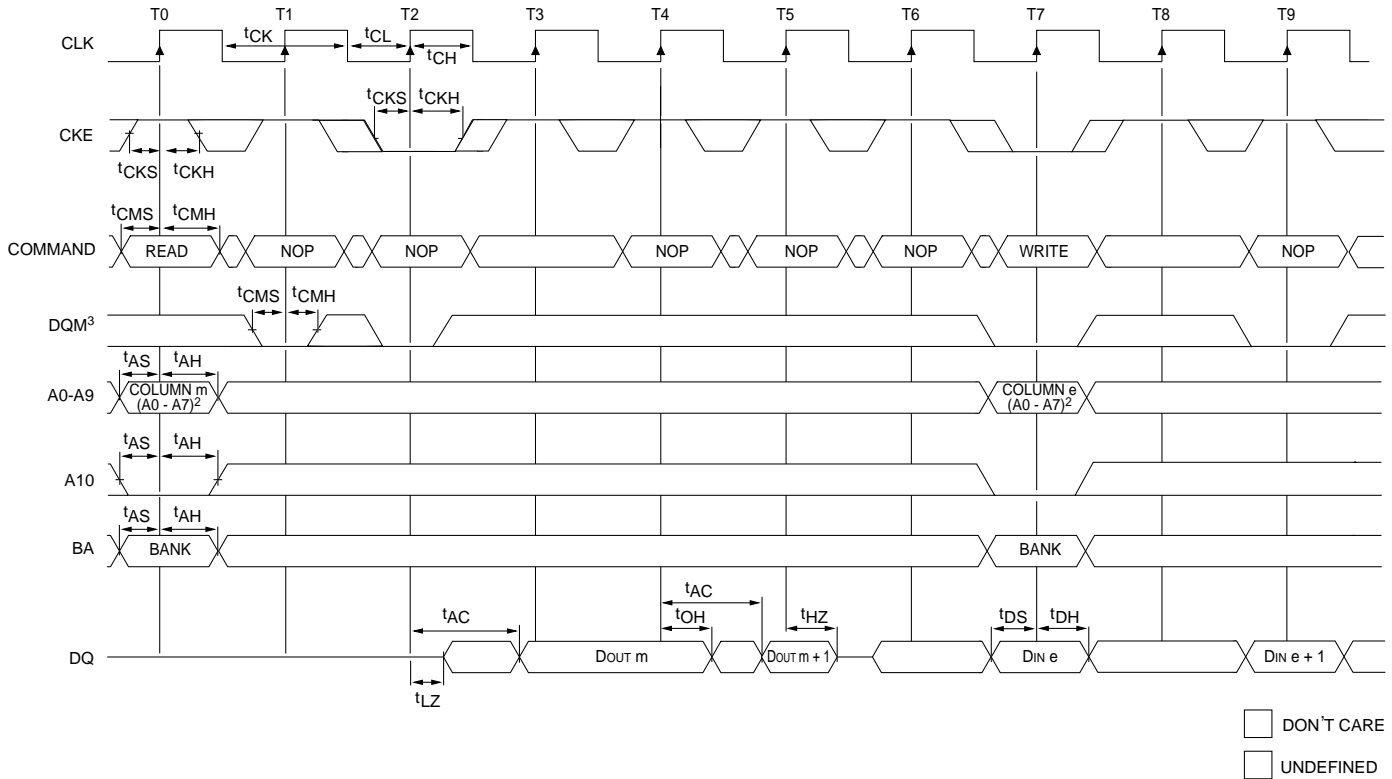
SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{AH}$	1		1		1		ns
$t_{AS}$	2		2		2		ns
$t_{CH}$	2.5		2.75		3		ns
$t_{CL}$	2.5		2.75		3		ns
$t_{CK} (3)$	6		7		8		ns
$t_{CK} (2)$	8		10		13		ns

SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{CK} (1)$	20		25		25		ns
$t_{CKH}$	1		1		1		ns
$t_{CKS}$	2		2		2		ns
$t_{CMH}$	1		1		1		ns
$t_{CMS}$	2		2		2		ns

\*CAS latency indicated in parentheses.

**NOTE:** 1. Violating refresh requirements during power-down may result in loss of data.  
 2. DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.

## CLOCK SUSPEND MODE <sup>1</sup>



□ DON'T CARE  
□ UNDEFINED

### TIMING PARAMETERS

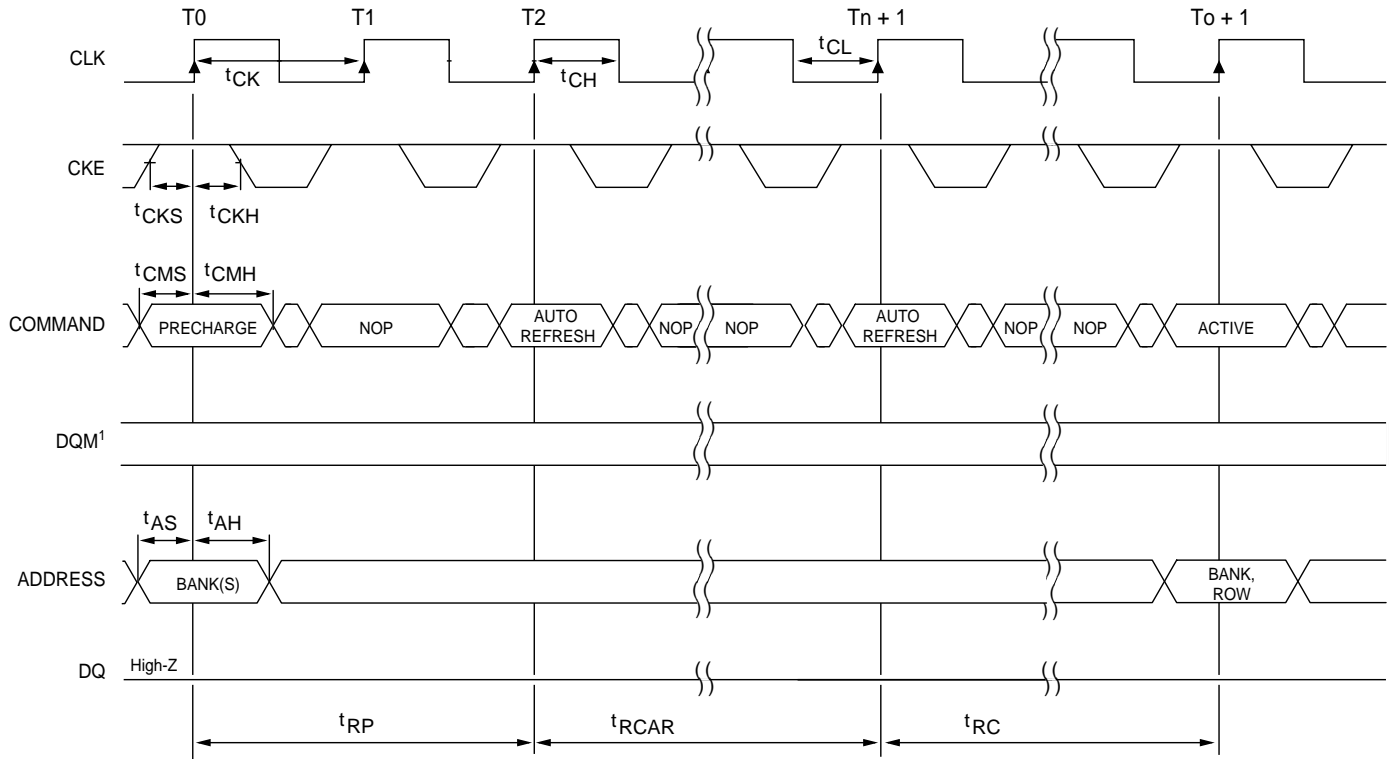
SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>AC</sub> (3)		5.5		5.5		6	ns
t <sub>AC</sub> (2)		8		8.5		9	ns
t <sub>AC</sub> (1)		18		22		22	ns
t <sub>AH</sub>	1		1		1		ns
t <sub>AS</sub>	2		2		2		ns
t <sub>CH</sub>	2.5		2.75		3		ns
t <sub>CL</sub>	2.5		2.75		3		ns
t <sub>CK</sub> (3)	6		7		8		ns
t <sub>CK</sub> (2)	8		10		13		ns
t <sub>CK</sub> (1)	20		25		25		ns
t <sub>CKH</sub>	1		1		1		ns

SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>CKS</sub>	2		2		2		ns
t <sub>CMH</sub>	1		1		1		ns
t <sub>CMS</sub>	2		2		2		ns
t <sub>DH</sub>	1		1		1		ns
t <sub>DS</sub>	2		2		2		ns
t <sub>HZ</sub> (3)		5.5		5.5		6	ns
t <sub>HZ</sub> (2)		6		8.5		9	ns
t <sub>HZ</sub> (1)		18		22		22	ns
t <sub>LZ</sub>	1		1		1		ns
t <sub>OH</sub>	1.5		1.5		1.5		ns

\*CAS latency indicated in parentheses.

**NOTE:** 1. For this example, the burst length = 2, the CAS latency = 3, and AUTO PRECHARGE is disabled.  
2. A8 and A9 = "Don't Care".  
3. DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.

## AUTO REFRESH MODE



Precharge all active banks.

□ DON'T CARE  
□ UNDEFINED

## TIMING PARAMETERS

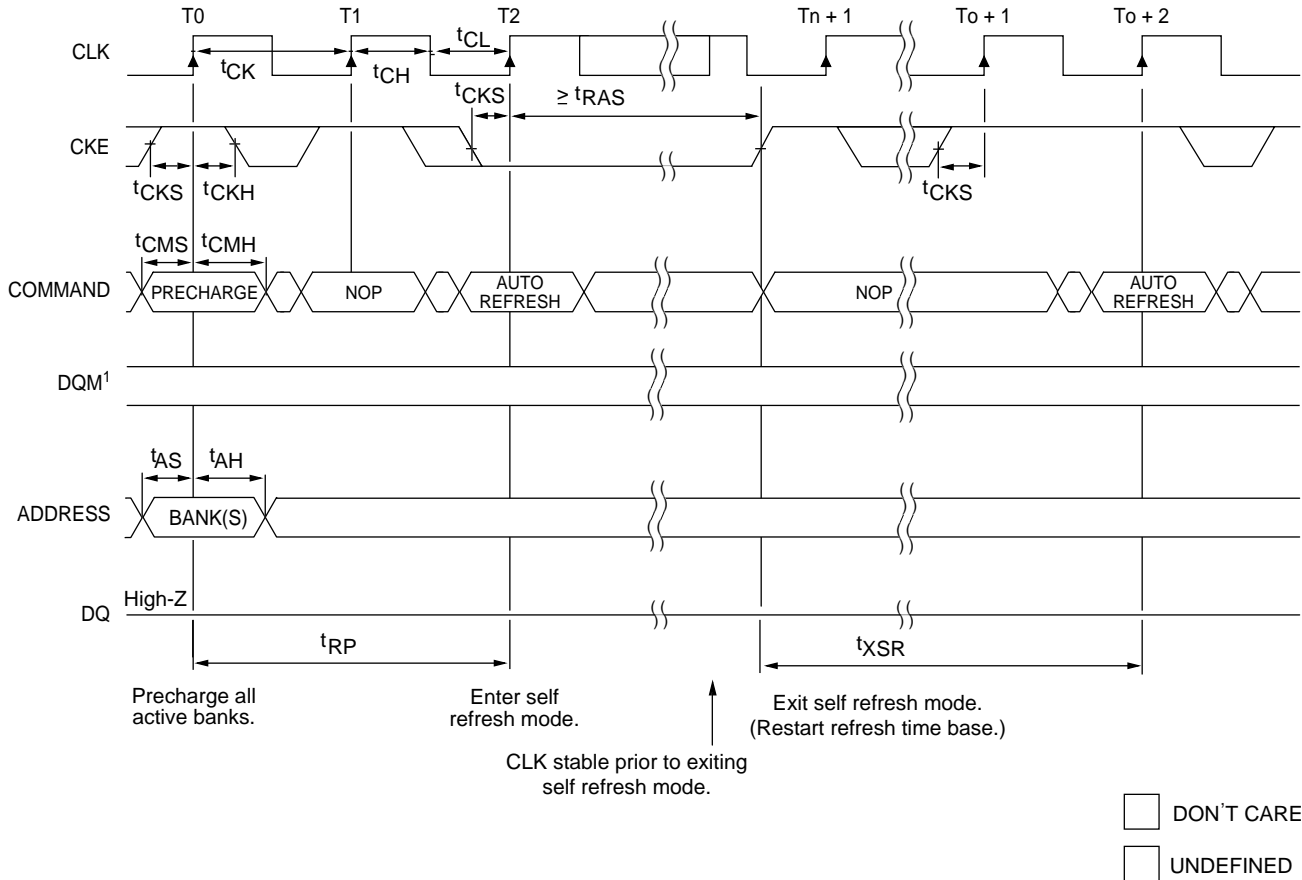
SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>AH</sub>	1		1		1		ns
t <sub>AS</sub>	2		2		2		ns
t <sub>CH</sub>	2.5		2.75		3		ns
t <sub>CL</sub>	2.5		2.75		3		ns
t <sub>CK</sub> (3)	6		7		8		ns
t <sub>CK</sub> (2)	8		10		13		ns
t <sub>CK</sub> (1)	20		25		25		ns

SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>CKH</sub>	1		1		1		ns
t <sub>CKS</sub>	2		2		2		ns
t <sub>CMH</sub>	1		1		1		ns
t <sub>CMS</sub>	2		2		2		ns
t <sub>RC</sub>	60		70		80		ns
t <sub>RCAR</sub>	66		70		80		ns
t <sub>RP</sub>	18		21		24		ns

\*CAS latency indicated in parentheses.

**NOTE:** 1. DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.

**SELF REFRESH MODE**



**TIMING PARAMETERS**

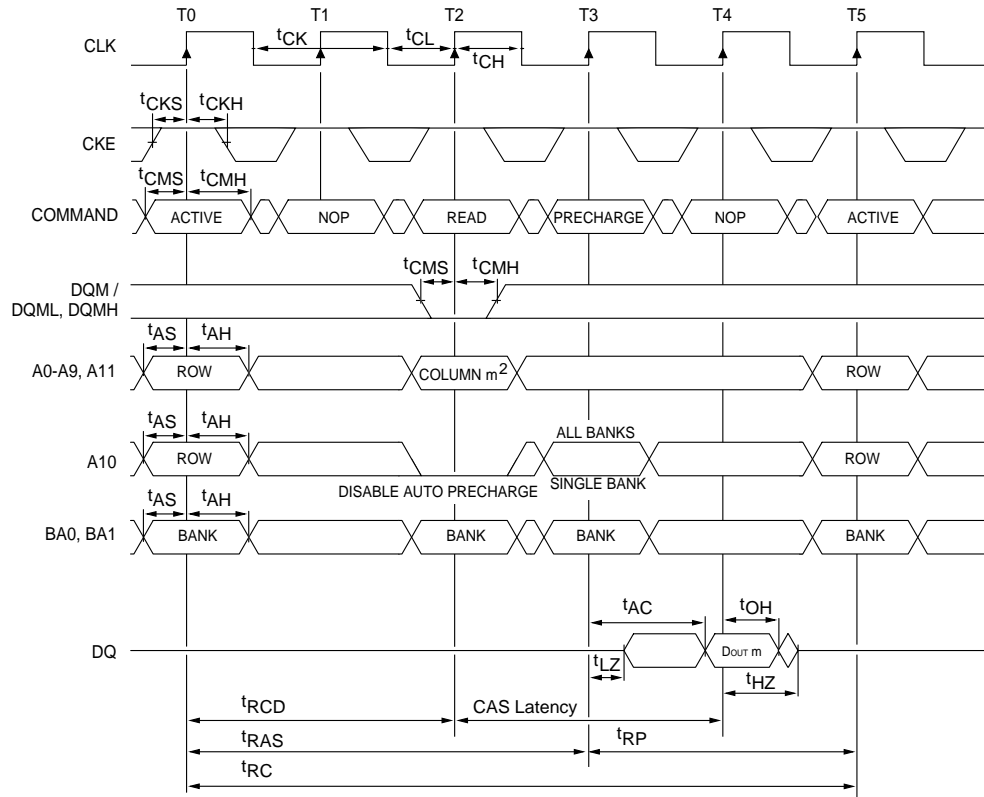
SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>AH</sub>	1		1		1		ns
t <sub>AS</sub>	2		2		2		ns
t <sub>CH</sub>	2.5		2.75		3		ns
t <sub>CL</sub>	2.5		2.75		3		ns
t <sub>CK</sub> (3)	6		7		8		ns
t <sub>CK</sub> (2)	8		10		13		ns
t <sub>CK</sub> (1)	20		25		25		ns

SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>CKH</sub>	1		1		1		ns
t <sub>CKS</sub>	2		2		2		ns
t <sub>CMH</sub>	1		1		1		ns
t <sub>CMS</sub>	2		2		2		ns
t <sub>RAS</sub>	42	120,000	42	120,000	48	120,000	ns
t <sub>RP</sub>	18		21		24		ns
t <sub>XSR</sub>	80		80		80		ns

\*CAS latency indicated in parentheses.

**NOTE:** 1. DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.

## SINGLE READ--WITHOUT AUTO PRECHARGE 1



□ DON'T CARE  
□ UNDEFINED

### TIMING PARAMETERS

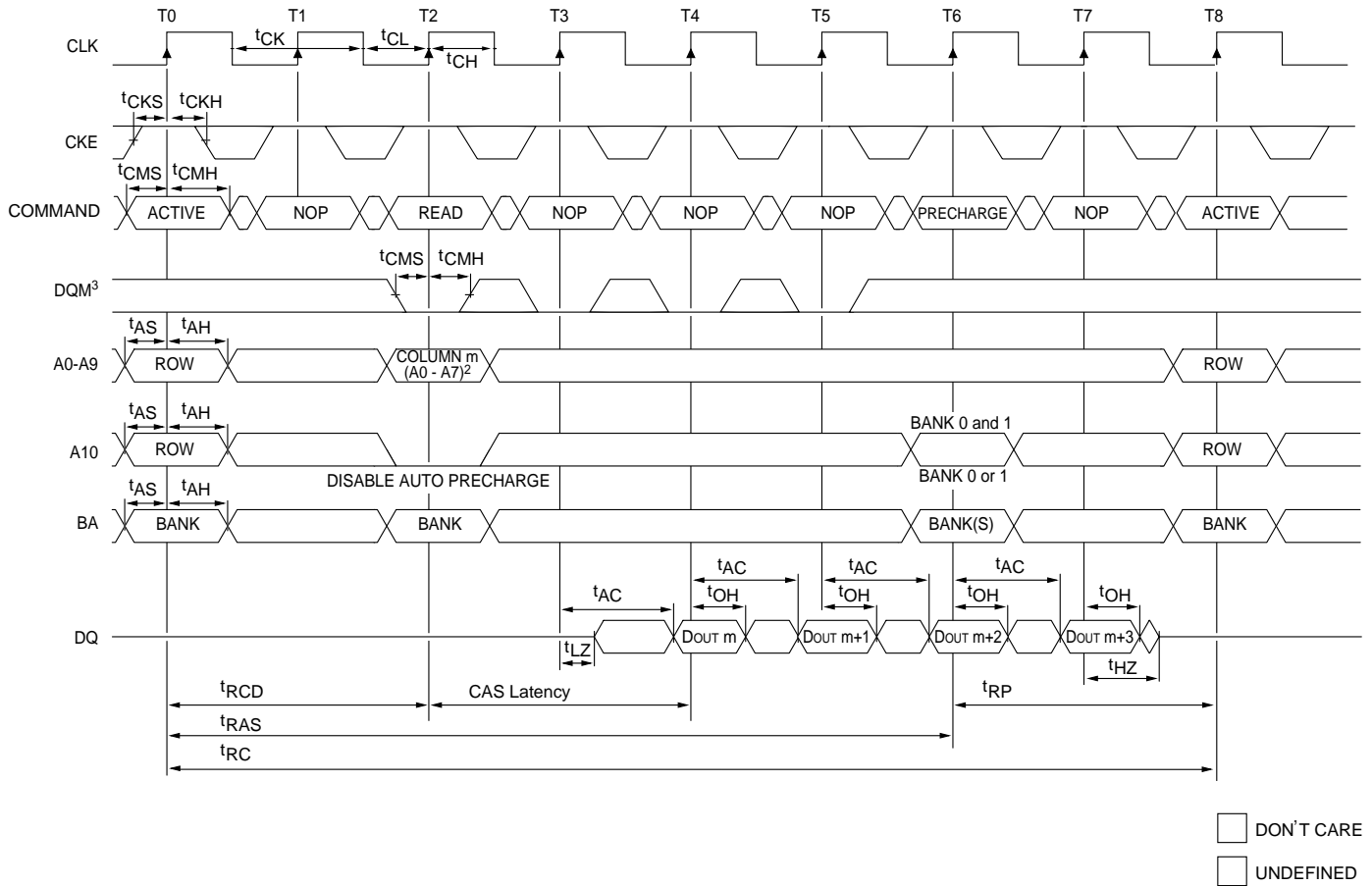
SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sup>'</sup> AC (3)		5.5		5.5		6	ns
t <sup>'</sup> AC (2)		8		8.5		9	ns
t <sup>'</sup> AC (1)		18		22		22	ns
t <sup>'</sup> AH	1		1		1		ns
t <sup>'</sup> AS	2		2		2		ns
t <sup>'</sup> CH	2.5		2.75		3		ns
t <sup>'</sup> CL	2.5		2.75		3		ns
t <sup>'</sup> CK (3)	6		7		8		ns
t <sup>'</sup> CK (2)	8		10		13		ns
t <sup>'</sup> CK (1)	20		25		25		ns
t <sup>'</sup> CKH	1		1		1		ns
t <sup>'</sup> CKS	2		2		2		ns

SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sup>'</sup> CMH	1		1		1		ns
t <sup>'</sup> CMS	2		2		2		ns
t <sup>'</sup> HZ (3)		5.5		5.5		6	ns
t <sup>'</sup> HZ (2)		6		8.5		9	ns
t <sup>'</sup> HZ (1)		18		22		22	ns
t <sup>'</sup> LZ	1		1		1		ns
t <sup>'</sup> OH	1.5		1.5		1.5		ns
t <sup>'</sup> RAS	42	120,000	42	120,000	48	120,000	ns
t <sup>'</sup> RC	60		70		80		ns
t <sup>'</sup> RCD	18		20		24		ns
t <sup>'</sup> RP	18		21		24		ns

\*CAS latency indicated in parentheses.

**NOTE:** 1. For this example, the burst length = 4, the CAS latency = 2, and the READ burst is followed by a "manual" PRECHARGE.  
2. A8, A9 = "Don't Care."

## READ--WITHOUT AUTO PRECHARGE <sup>1</sup>



### TIMING PARAMETERS

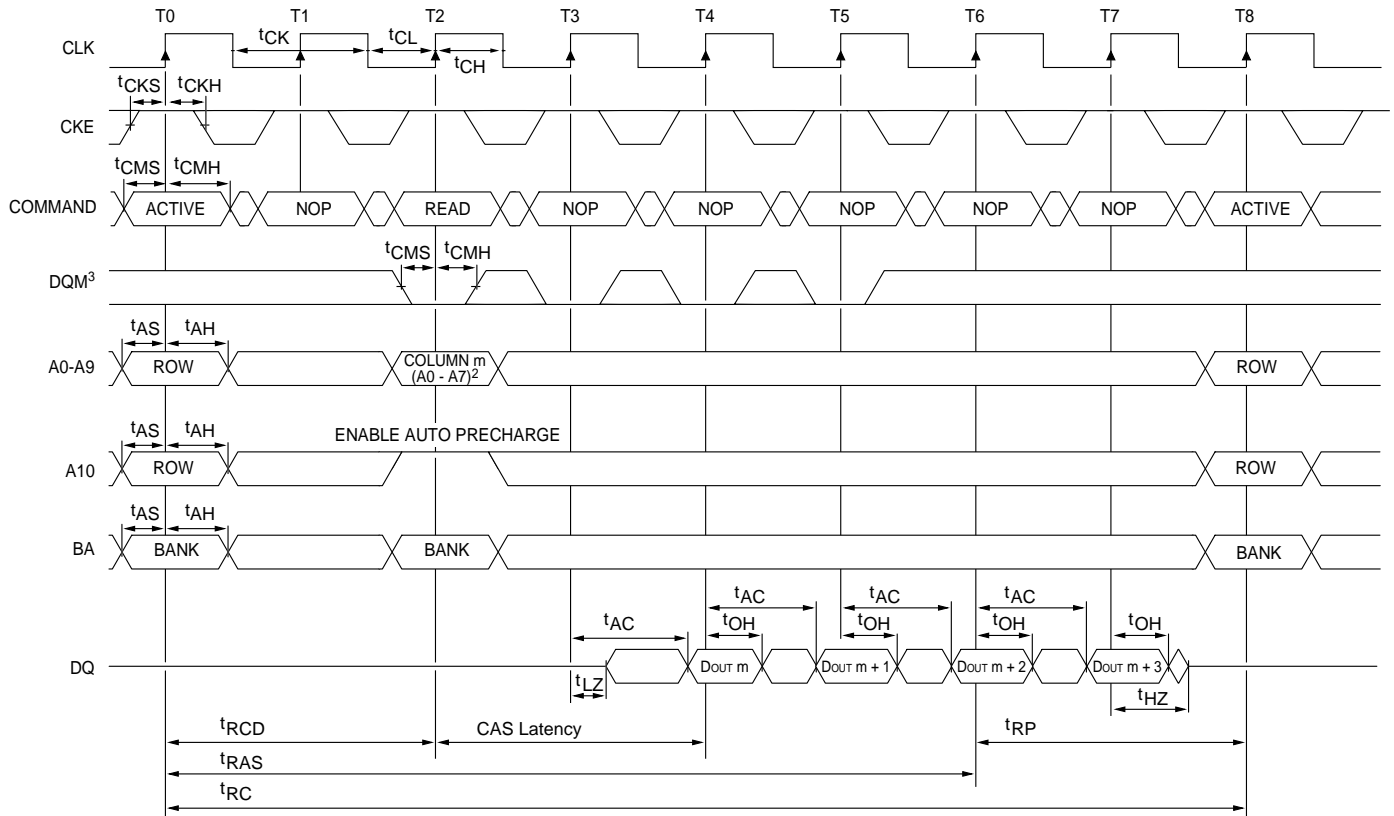
SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sup>AC</sup> (3)		5.5		5.5		6	ns
t <sup>AC</sup> (2)		8		8.5		9	ns
t <sup>AC</sup> (1)		18		22		22	ns
t <sup>AH</sup>	1		1		1		ns
t <sup>AS</sup>	2		2		2		ns
t <sup>CH</sup>	2.5		2.75		3		ns
t <sup>CL</sup>	2.5		2.75		3		ns
t <sup>CK</sup> (3)	6		7		8		ns
t <sup>CK</sup> (2)	8		10		13		ns
t <sup>CK</sup> (1)	20		25		25		ns
t <sup>CKH</sup>	1		1		1		ns
t <sup>CKS</sup>	2		2		2		ns

SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sup>CMH</sup>	1		1		1		ns
t <sup>CMS</sup>	2		2		2		ns
t <sup>HZ</sup> (3)		5.5		5.5		6	ns
t <sup>HZ</sup> (2)		6		8.5		9	ns
t <sup>HZ</sup> (1)		18		22		22	ns
t <sup>LZ</sup>	1		1		1		ns
t <sup>OH</sup>	1.5		1.5		1.5		ns
t <sup>RAS</sup>	42	120,000	42	120,000	48	120,000	ns
t <sup>RC</sup>	60		70		80		ns
t <sup>RCD</sup>	18		20		24		ns
t <sup>RP</sup>	18		21		24		ns

\*CAS latency indicated in parentheses.

- NOTE:**
1. For this example, the burst length = 4, the CAS latency = 2, and the READ burst is followed by a "manual" PRECHARGE.
  2. A8 and A9 = "Don't Care."
  3. DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.

## READ--WITH AUTO PRECHARGE 1



DON'T CARE  
 UNDEFINED

### TIMING PARAMETERS

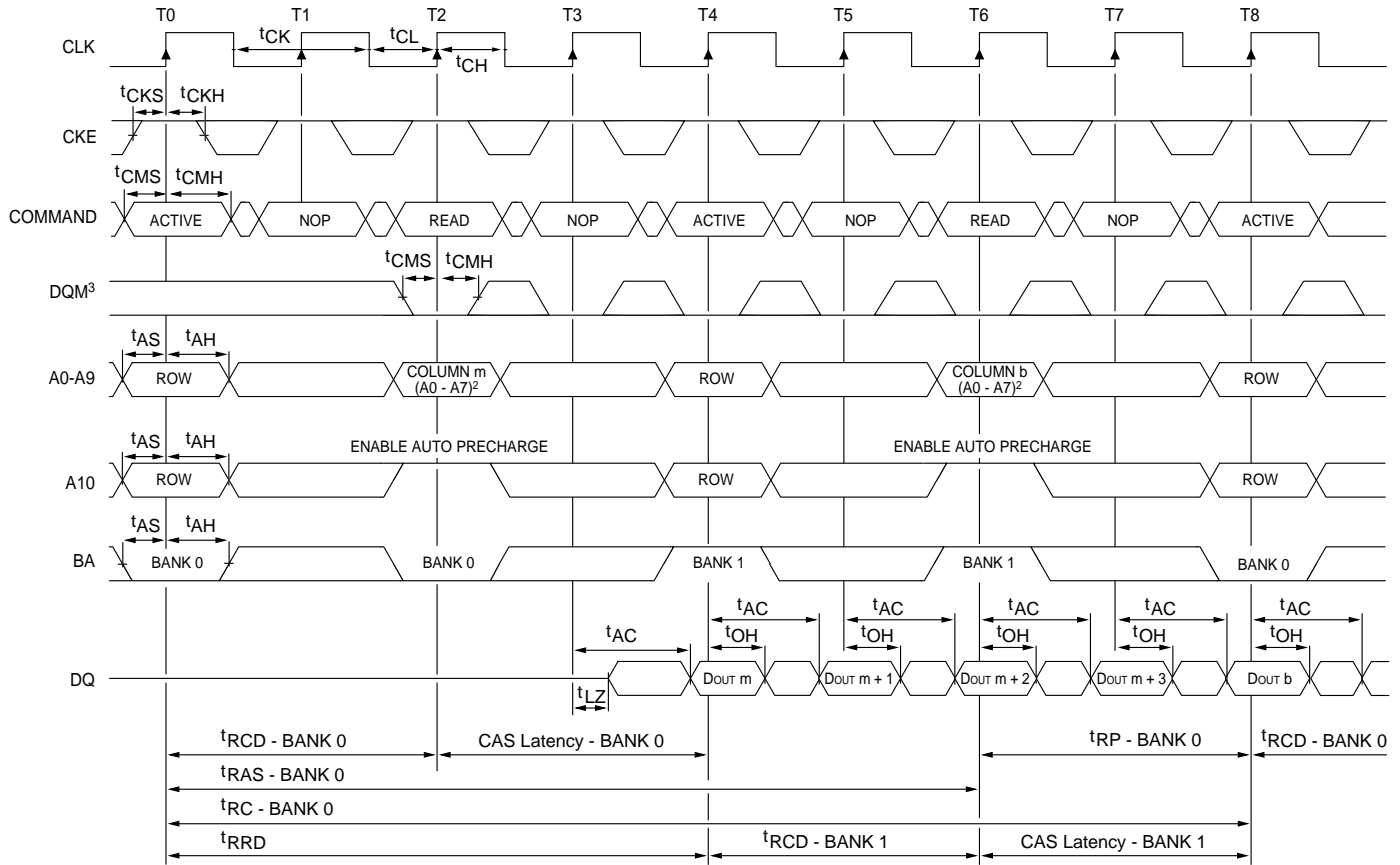
SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>AC</sub> (3)		5.5		5.5		6	ns
t <sub>AC</sub> (2)		8		8.5		9	ns
t <sub>AC</sub> (1)		18		22		22	ns
t <sub>AH</sub>	1		1		1		ns
t <sub>AS</sub>	2		2		2		ns
t <sub>CH</sub>	2.5		2.75		3		ns
t <sub>CL</sub>	2.5		2.75		3		ns
t <sub>CK</sub> (3)	6		7		8		ns
t <sub>CK</sub> (2)	8		10		13		ns
t <sub>CK</sub> (1)	20		25		25		ns
t <sub>CKH</sub>	1		1		1		ns
t <sub>CKS</sub>	2		2		2		ns

SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>CMH</sub>	1		1		1		ns
t <sub>CMS</sub>	2		2		2		ns
t <sub>HZ</sub> (3)		5.5		5.5		6	ns
t <sub>HZ</sub> (2)		6		8.5		9	ns
t <sub>HZ</sub> (1)		18		22		22	ns
t <sub>LZ</sub>	1		1		1		ns
t <sub>OH</sub>	1.5		1.5		1.5		ns
t <sub>RAS</sub>	42	120,000	42	120,000	48	120,000	ns
t <sub>RC</sub>	60		70		80		ns
t <sub>RCD</sub>	18		20		24		ns
t <sub>RP</sub>	18		21		24		ns

\*CAS latency indicated in parentheses.

- NOTE:**
1. For this example, the burst length = 4, and the CAS latency = 2.
  2. A8 and A9 = "Don't Care."
  3. DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.

## ALTERNATING BANK READ ACCESSES 1



DON'T CARE  
 UNDEFINED

### TIMING PARAMETERS

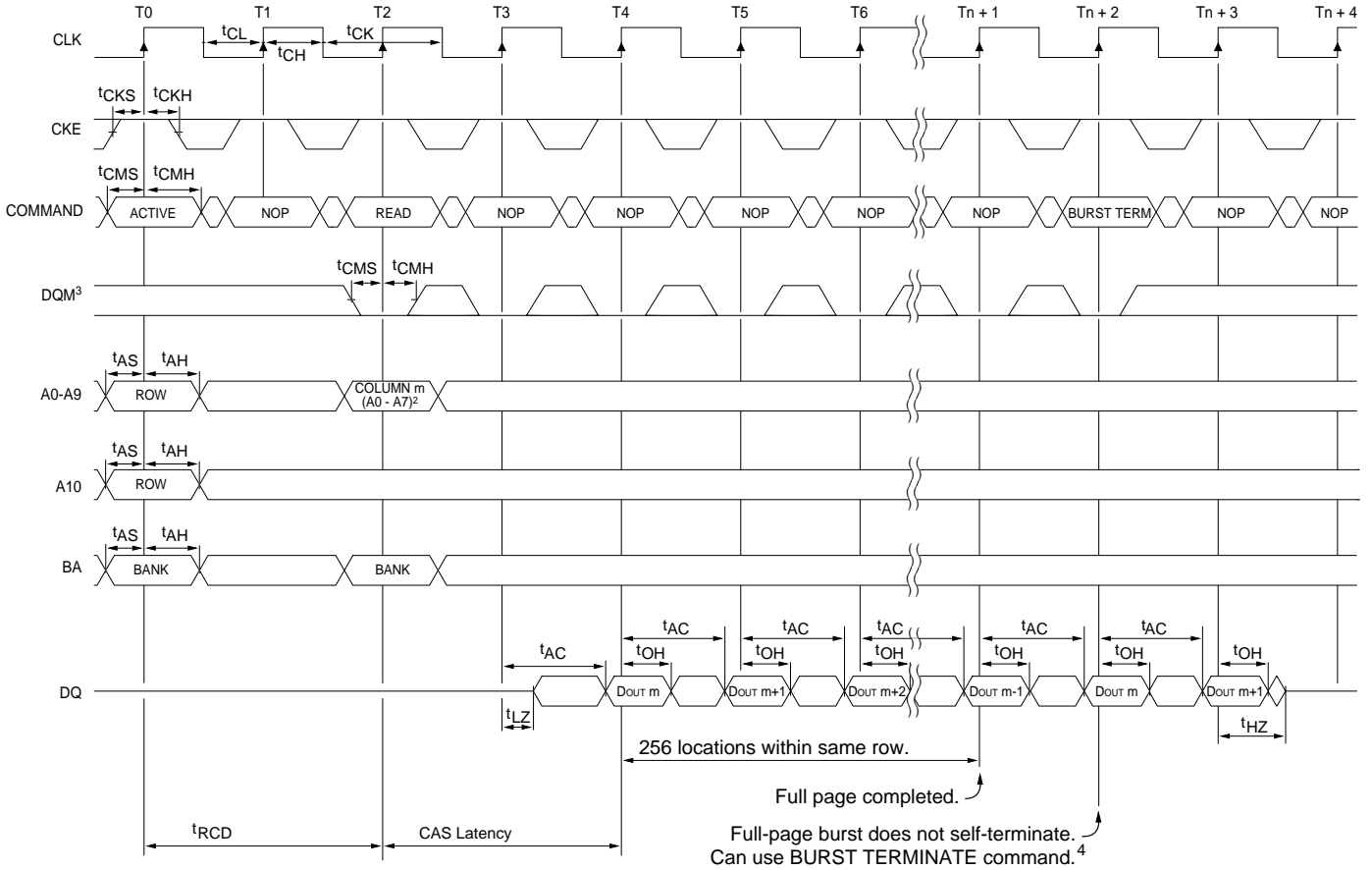
SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>AC</sub> (3)		5.5		5.5		6	ns
t <sub>AC</sub> (2)		8		8.5		9	ns
t <sub>AC</sub> (1)		18		22		22	ns
t <sub>AH</sub>	1		1		1		ns
t <sub>AS</sub>	2		2		2		ns
t <sub>CH</sub>	2.5		2.75		3		ns
t <sub>CL</sub>	2.5		2.75		3		ns
t <sub>CK</sub> (3)	6		7		8		ns
t <sub>CK</sub> (2)	8		10		13		ns
t <sub>CK</sub> (1)	20		25		25		ns
t <sub>CKH</sub>	1		1		1		ns

SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>CKS</sub>	2		2		2		ns
t <sub>CMH</sub>	1		1		1		ns
t <sub>CMS</sub>	2		2		2		ns
t <sub>LZ</sub>	1		1		1		ns
t <sub>OH</sub>	1.5		1.5		1.5		ns
t <sub>RAS</sub>	42	120,000	42	120,000	48	120,000	ns
t <sub>RC</sub>	60		70		80		ns
t <sub>RCD</sub>	18		20		24		ns
t <sub>RP</sub>	18		21		24		ns
t <sub>RRD</sub>	12		14		16		ns

\*CAS latency indicated in parentheses.

- NOTE:**
1. For this example, the burst length = 4, and the CAS latency = 2.
  2. A8 and A9 = "Don't Care."
  3. DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.

## READ--FULL-PAGE BURST <sup>1</sup>



□ DON'T CARE  
□ UNDEFINED

### TIMING PARAMETERS

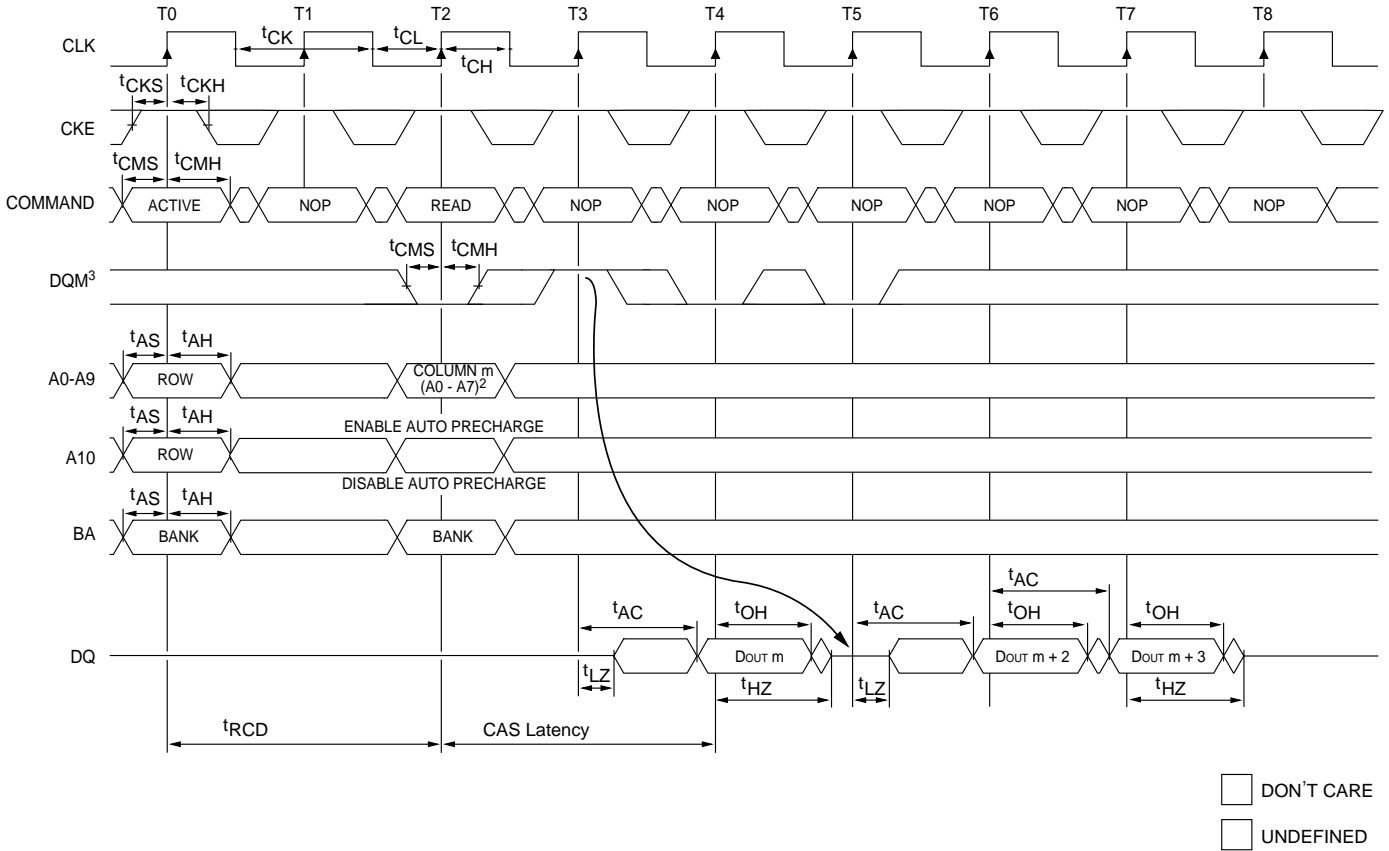
SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
<sup>1</sup> tAC (3)		5.5		5.5		6	ns
<sup>1</sup> tAC (2)		8		8.5		9	ns
<sup>1</sup> tAC (1)		18		22		22	ns
<sup>1</sup> tAH	1		1		1		ns
<sup>1</sup> tAS	2		2		2		ns
<sup>1</sup> tCH	2.5		2.75		3		ns
<sup>1</sup> tCL	2.5		2.75		3		ns
<sup>1</sup> tCK (3)	6		7		8		ns
<sup>1</sup> tCK (2)	8		10		13		ns
<sup>1</sup> tCK (1)	20		25		25		ns

SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
<sup>1</sup> tCKH	1		1		1		ns
<sup>1</sup> tCKS	2		2		2		ns
<sup>1</sup> tCMH	1		1		1		ns
<sup>1</sup> tCMS	2		2		2		ns
<sup>1</sup> tHZ (3)		5.5		5.5		6	ns
<sup>1</sup> tHZ (2)		6		8.5		9	ns
<sup>1</sup> tHZ (1)		18		22		22	ns
<sup>1</sup> tLZ	1		1		1		ns
<sup>1</sup> tOH	1.5		1.5		1.5		ns
<sup>1</sup> tRCD	18		20		24		ns

\*CAS latency indicated in parentheses.

- NOTE:**
1. For this example, the CAS latency = 2.
  2. A8 and A9 = "Don't Care."
  3. DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.
  4. Page left open; no <sup>1</sup>RP.

## READ--DQM OPERATION <sup>1</sup>



### TIMING PARAMETERS

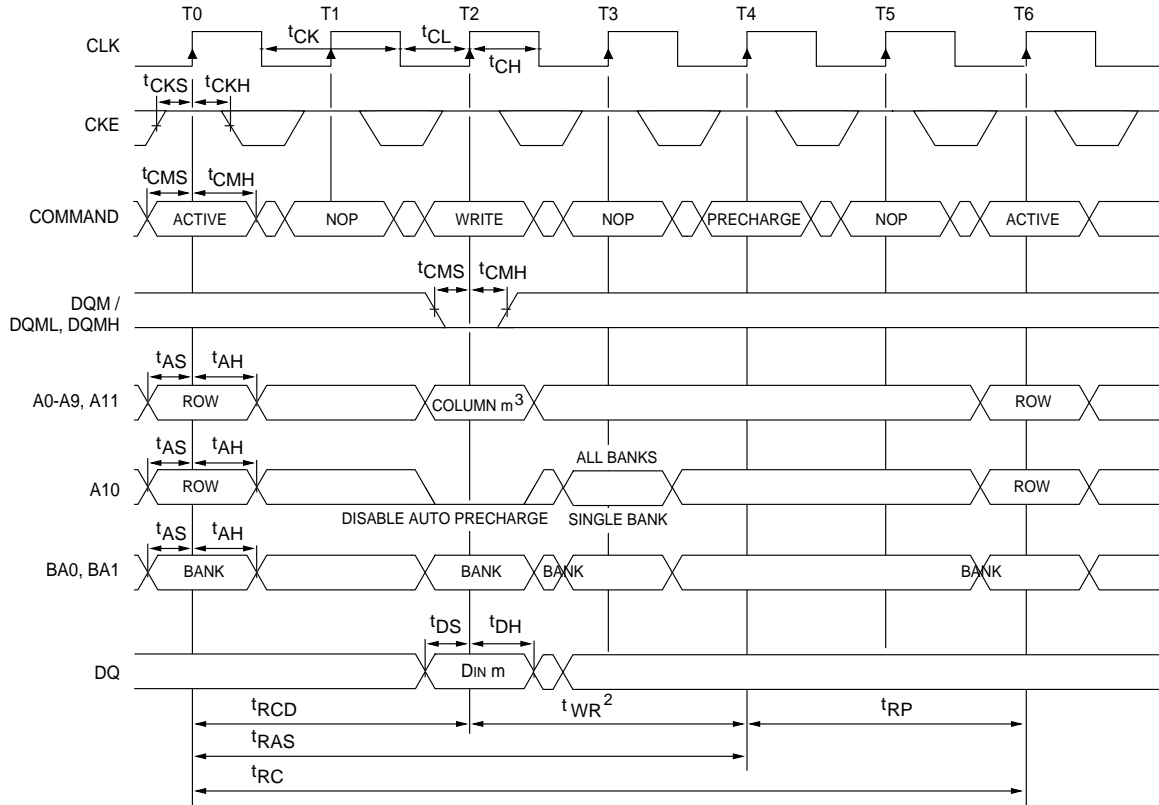
SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>AC</sub> (3)		5.5		5.5		6	ns
t <sub>AC</sub> (2)		8		8.5		9	ns
t <sub>AC</sub> (1)		18		22		22	ns
t <sub>AH</sub>	1		1		1		ns
t <sub>AS</sub>	2		2		2		ns
t <sub>CH</sub>	2.5		2.75		3		ns
t <sub>CL</sub>	2.5		2.75		3		ns
t <sub>CK</sub> (3)	6		7		8		ns
t <sub>CK</sub> (2)	8		10		13		ns
t <sub>CK</sub> (1)	20		25		25		ns

SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>CKH</sub>	1		1		1		ns
t <sub>CKS</sub>	2		2		2		ns
t <sub>CMH</sub>	1		1		1		ns
t <sub>CMS</sub>	2		2		2		ns
t <sub>HZ</sub> (3)		5.5		5.5		6	ns
t <sub>HZ</sub> (2)		6		8.5		9	ns
t <sub>HZ</sub> (1)		18		22		22	ns
t <sub>LZ</sub>	1		1		1		ns
t <sub>OH</sub>	1.5		1.5		1.5		ns
t <sub>RCD</sub>	18		20		24		ns

\*CAS latency indicated in parentheses.

- NOTE:**
1. For this example, the burst length = 4, and the CAS latency = 2.
  2. A8 and A9 = "Don't Care."
  3. DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.

## SINGLE WRITE--WITHOUT AUTO PRECHARGE <sup>1</sup>



DON'T CARE  
 UNDEFINED

### TIMING PARAMETERS

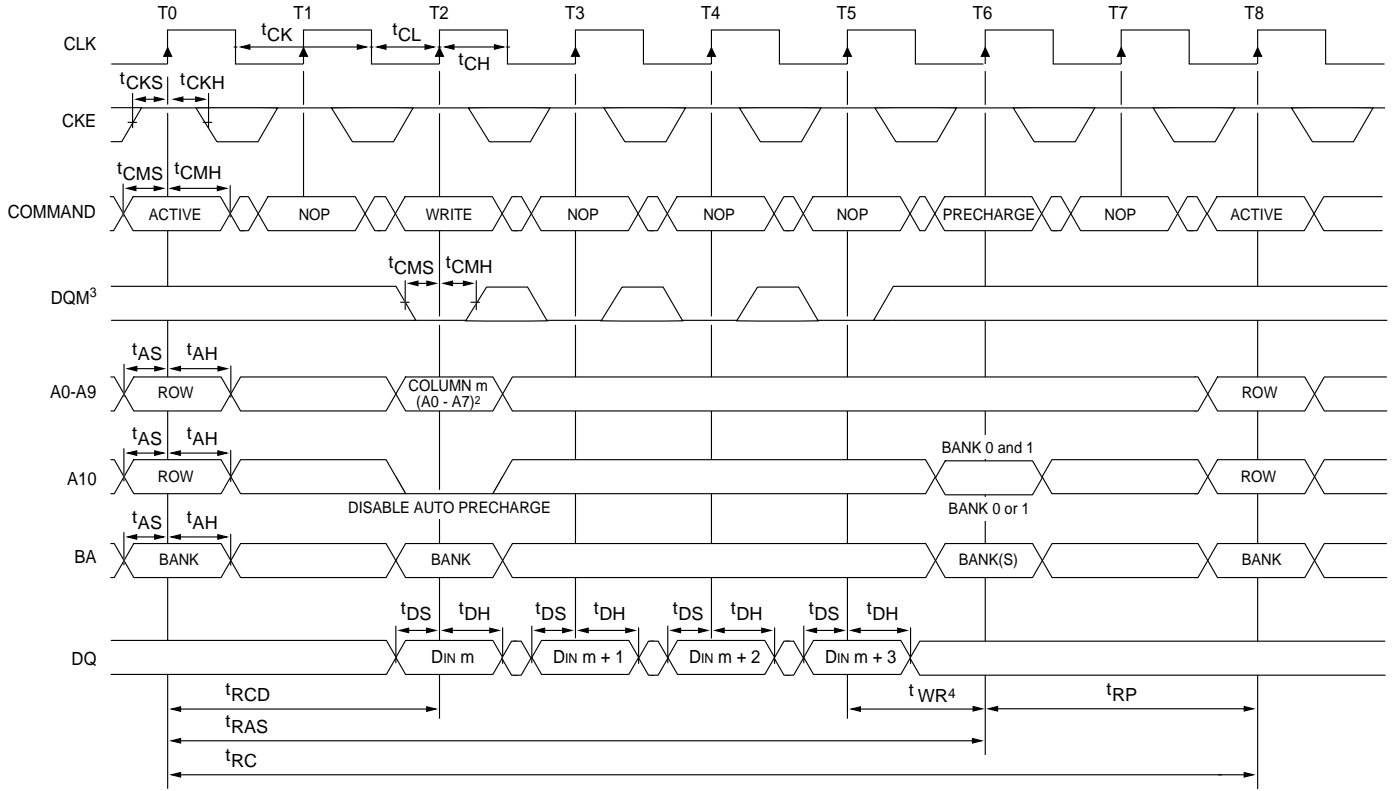
SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>AH</sub>	1		1		1		ns
t <sub>AS</sub>	2		2		2		ns
t <sub>CH</sub>	2.5		2.75		3		ns
t <sub>CL</sub>	2.5		2.75		3		ns
t <sub>CK</sub> (3)	6		7		8		ns
t <sub>CK</sub> (2)	8		10		13		ns
t <sub>CK</sub> (1)	20		25		25		ns
t <sub>CKH</sub>	1		1		1		ns
t <sub>CKS</sub>	2		2		2		ns

SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>CMH</sub>	1		1		1		ns
t <sub>CMS</sub>	2		2		2		ns
t <sub>DH</sub>	1		1		1		ns
t <sub>DS</sub>	2		2		2		ns
t <sub>RAS</sub>	42	120,000	42	120,000	48	120,000	ns
t <sub>RC</sub>	60		70		80		ns
t <sub>RCD</sub>	18		20		24		ns
t <sub>RP</sub>	18		21		24		ns
t <sub>WR</sub>	10		10		10		ns

\*CAS latency indicated in parentheses.

- NOTE:**
1. For this example, the burst length = 4, and the WRITE burst is followed by a "manual" PRECHARGE.
  2. 10ns is required between <D<sub>IN m</sub>> and the PRECHARGE command, regardless of frequency, to meet t<sub>WR</sub>.
  3. A8, A9 = "Don't Care".

## WRITE--WITHOUT AUTO PRECHARGE <sup>1</sup>



DON'T CARE  
 UNDEFINED

### TIMING PARAMETERS

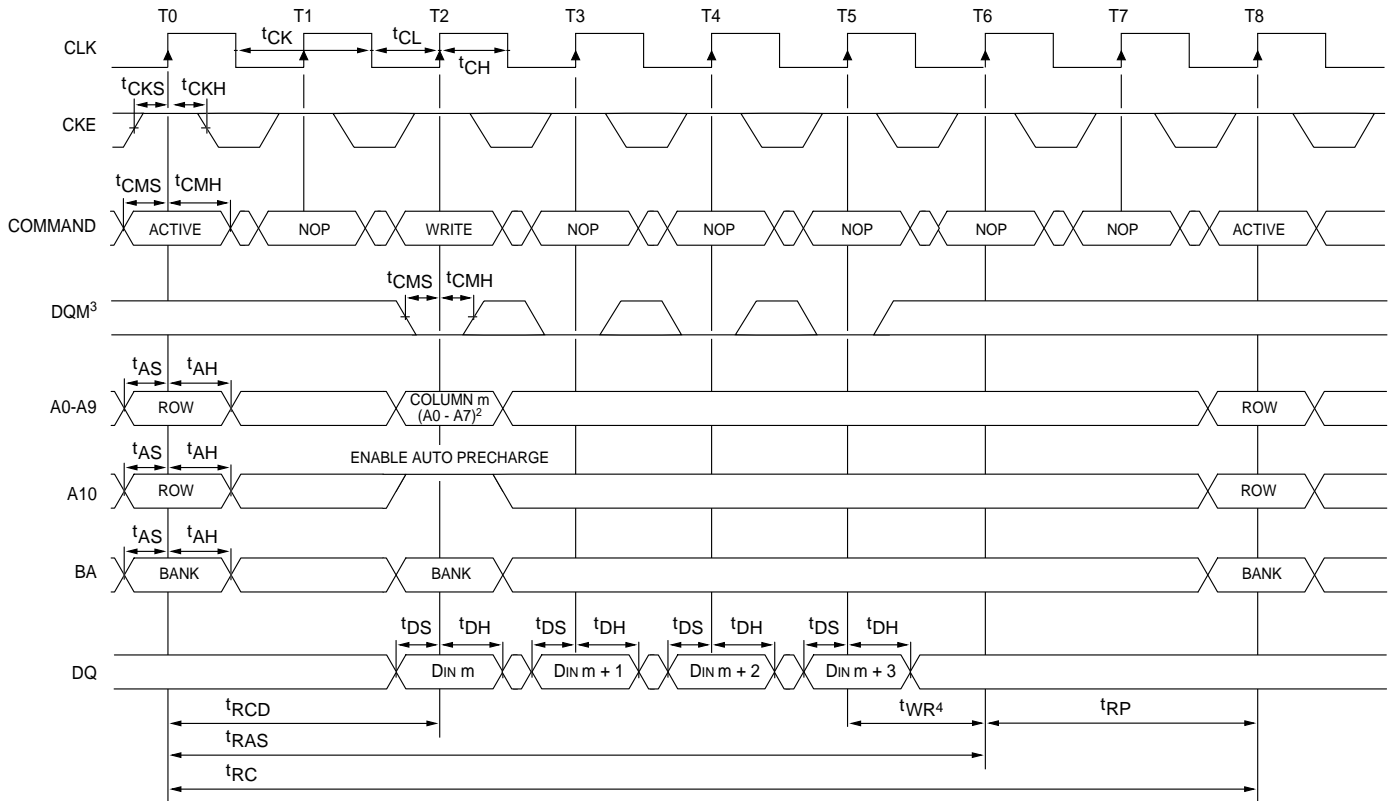
SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>AH</sub>	1		1		1		ns
t <sub>AS</sub>	2		2		2		ns
t <sub>CH</sub>	2.5		2.75		3		ns
t <sub>CL</sub>	2.5		2.75		3		ns
t <sub>CK (3)</sub>	6		7		8		ns
t <sub>CK (2)</sub>	8		10		13		ns
t <sub>CK (1)</sub>	20		25		25		ns
t <sub>CKH</sub>	1		1		1		ns
t <sub>CKS</sub>	2		2		2		ns

SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>CMH</sub>	1		1		1		ns
t <sub>CMS</sub>	2		2		2		ns
t <sub>DH</sub>	1		1		1		ns
t <sub>DS</sub>	2		2		2		ns
t <sub>RAS</sub>	42	120,000	42	120,000	48	120,000	ns
t <sub>RC</sub>	60		70		80		ns
t <sub>RCD</sub>	18		20		24		ns
t <sub>RP</sub>	18		21		24		ns
t <sub>WR</sub>	10		10		10		ns

\*CAS latency indicated in parentheses.

- NOTE:**
1. For this example, the burst length = 4, and the WRITE burst is followed by "manual" PRECHARGE.
  2. A8 and A9 = "Don't Care"
  3. DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.
  4. Faster frequencies will require two clocks (when t<sub>WR</sub> > t<sub>CK</sub>).

## WRITE--WITH AUTO PRECHARGE 1



DON'T CARE  
 UNDEFINED

### TIMING PARAMETERS

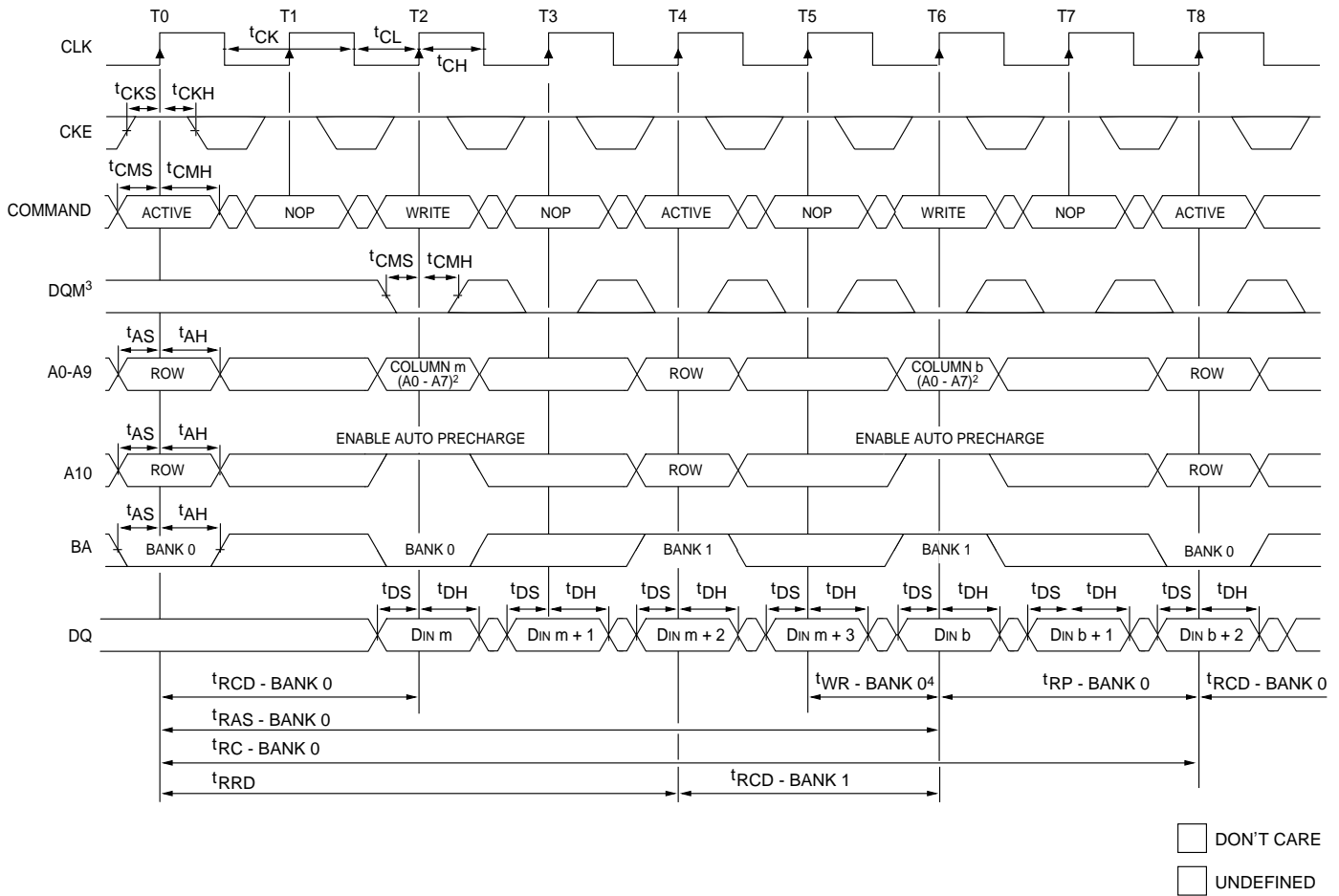
SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>AH</sub>	1		1		1		ns
t <sub>AS</sub>	2		2		2		ns
t <sub>CH</sub>	2.5		2.75		3		ns
t <sub>CL</sub>	2.5		2.75		3		ns
t <sub>CK</sub> (3)	6		7		8		ns
t <sub>CK</sub> (2)	8		10		13		ns
t <sub>CK</sub> (1)	20		25		25		ns
t <sub>CKH</sub>	1		1		1		ns
t <sub>CKS</sub>	2		2		2		ns

SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>CMH</sub>	1		1		1		ns
t <sub>CMS</sub>	2		2		2		ns
t <sub>DH</sub>	1		1		1		ns
t <sub>DS</sub>	2		2		2		ns
t <sub>RAS</sub>	42	120,000	42	120,000	48	120,000	ns
t <sub>RC</sub>	60		70		80		ns
t <sub>RCD</sub>	18		20		24		ns
t <sub>RP</sub>	18		21		24		ns
t <sub>WR</sub>	1 + 4ns		1 + 3ns		1 + 2ns		t <sub>CK</sub>

\*CAS latency indicated in parentheses.

- NOTE:**
1. For this example, the burst length = 4.
  2. A8 and A9 = "Don't Care"
  3. DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.
  4. Faster frequencies will require two clocks (when t<sub>WR</sub> > t<sub>CK</sub>).

## ALTERNATING BANK WRITE ACCESSES <sup>1</sup>



### TIMING PARAMETERS

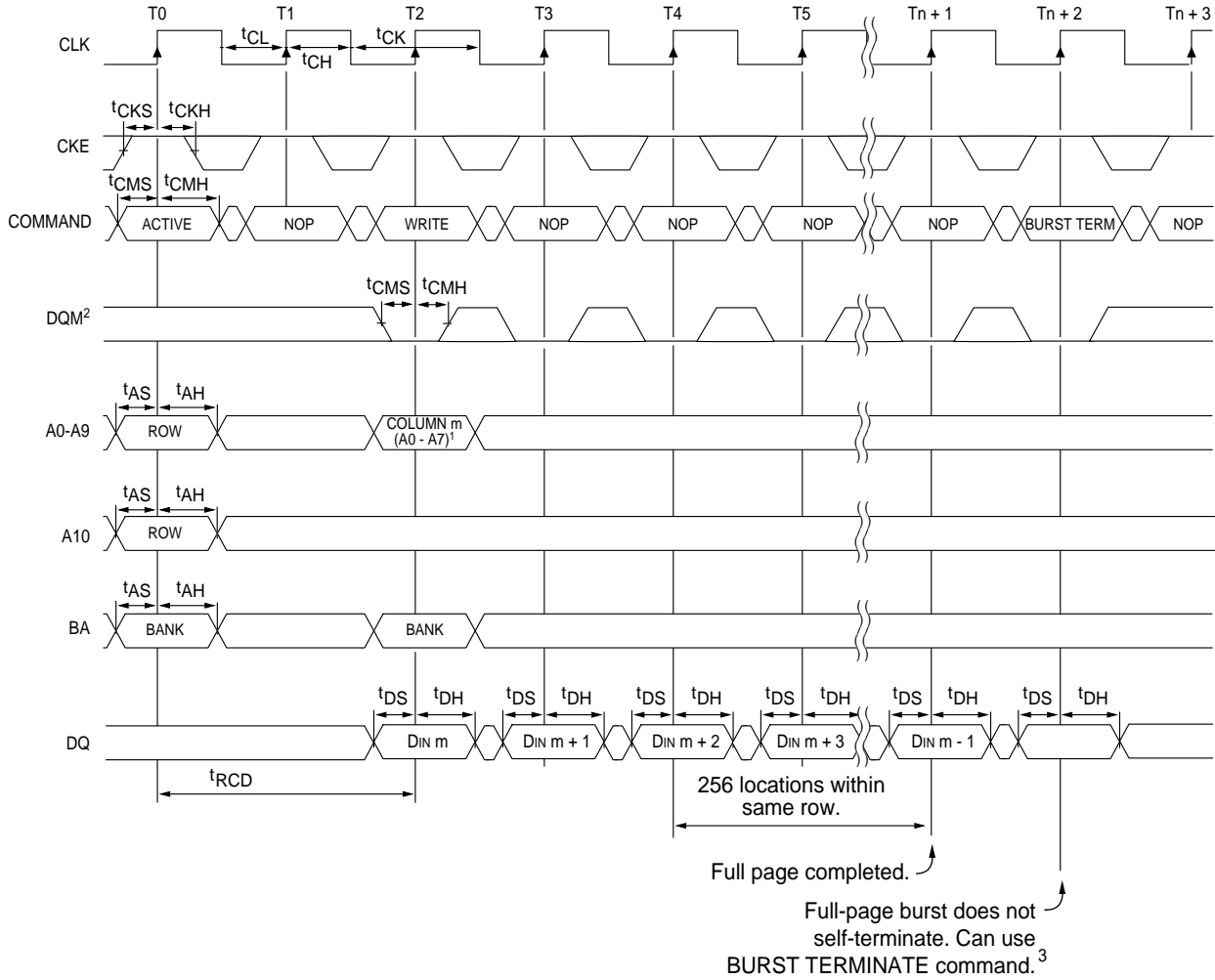
SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>AH</sub>	1		1		1		ns
t <sub>AS</sub>	2		2		2		ns
t <sub>CH</sub>	2.5		2.75		3		ns
t <sub>CL</sub>	2.5		2.75		3		ns
t <sub>CK</sub> (3)	6		7		8		ns
t <sub>CK</sub> (2)	8		10		13		ns
t <sub>CK</sub> (1)	20		25		25		ns
t <sub>CKH</sub>	1		1		1		ns
t <sub>CKS</sub>	2		2		2		ns
t <sub>CMH</sub>	1		1		1		ns

SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>CMS</sub>	2		2		2		ns
t <sub>DH</sub>	1		1		1		ns
t <sub>DS</sub>	2		2		2		ns
t <sub>RAS</sub>	42	120,000	42	120,000	48	120,000	ns
t <sub>RC</sub>	60		70		80		ns
t <sub>RCD</sub>	18		20		24		ns
t <sub>RP</sub>	18		21		24		ns
t <sub>RRD</sub>	12		14		16		ns
t <sub>WR</sub>	1 + 4ns		1 + 3ns		1 + 2ns		t <sub>CK</sub>

\*CAS latency indicated in parentheses.

- NOTE:**
1. For this example, the burst length = 4.
  2. A8 and A9 = "Don't Care"
  3. DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.
  4. Faster frequencies will require two clocks (when t<sub>WR</sub> > t<sub>CK</sub>).

## WRITE--FULL-PAGE BURST



DON'T CARE  
 UNDEFINED

### TIMING PARAMETERS

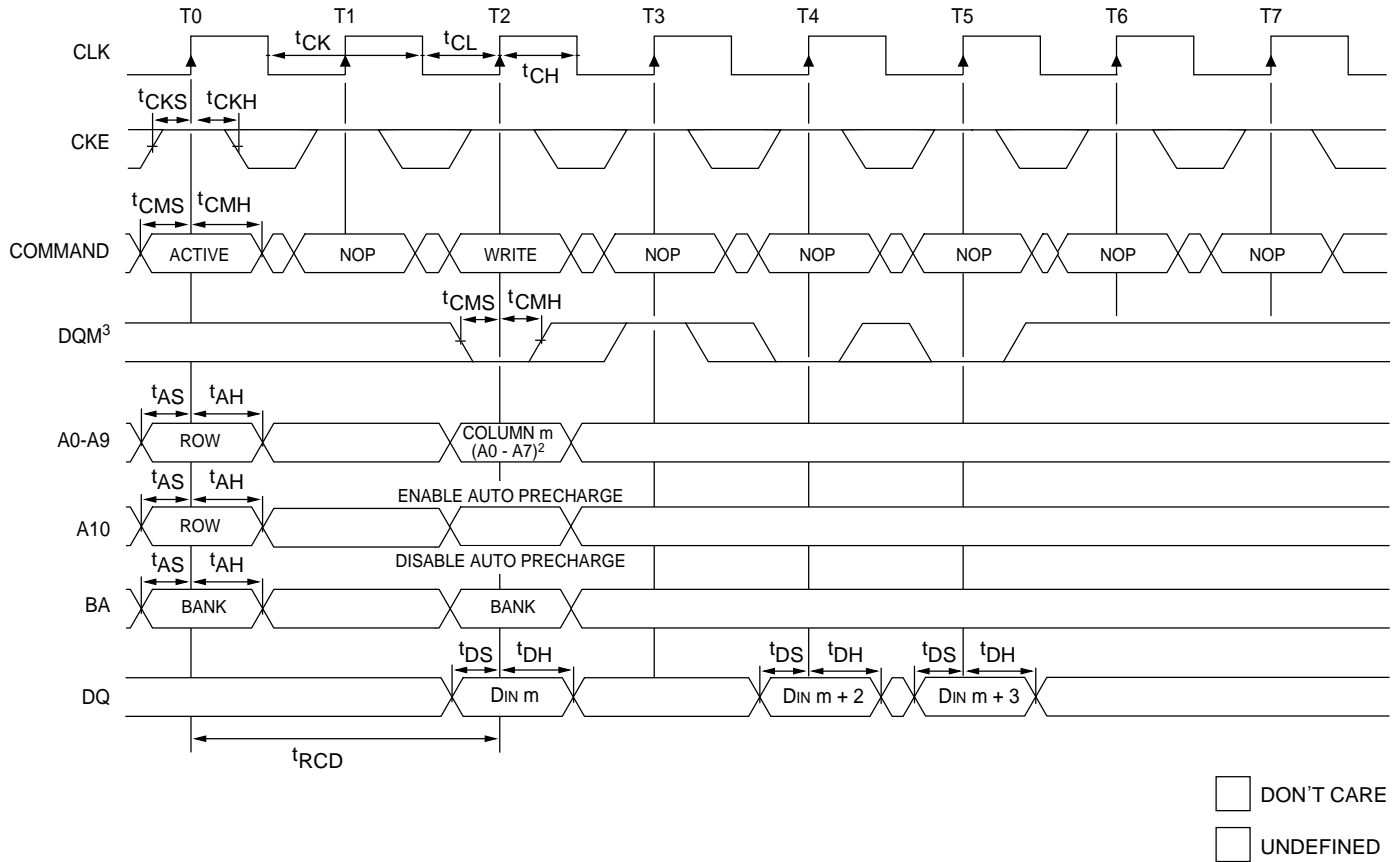
SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>AH</sub>	1		1		1		ns
t <sub>AS</sub>	2		2		2		ns
t <sub>CH</sub>	2.5		2.75		3		ns
t <sub>CL</sub>	2.5		2.75		3		ns
t <sub>CK (3)</sub>	6		7		8		ns
t <sub>CK (2)</sub>	8		10		13		ns
t <sub>CK (1)</sub>	20		25		25		ns

SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>CKH</sub>	1		1		1		ns
t <sub>CKS</sub>	2		2		2		ns
t <sub>CMH</sub>	1		1		1		ns
t <sub>CMS</sub>	2		2		2		ns
t <sub>DH</sub>	1		1		1		ns
t <sub>DS</sub>	2		2		2		ns
t <sub>RCD</sub>	18		20		24		ns

\*CAS latency indicated in parentheses.

- NOTE:**
1. A8 and A9 = "Don't Care."
  2. DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.
  3. Page left open; no t<sub>RP</sub>.

## WRITE--DQM OPERATION <sup>1</sup>



□ DON'T CARE  
□ UNDEFINED

## TIMING PARAMETERS

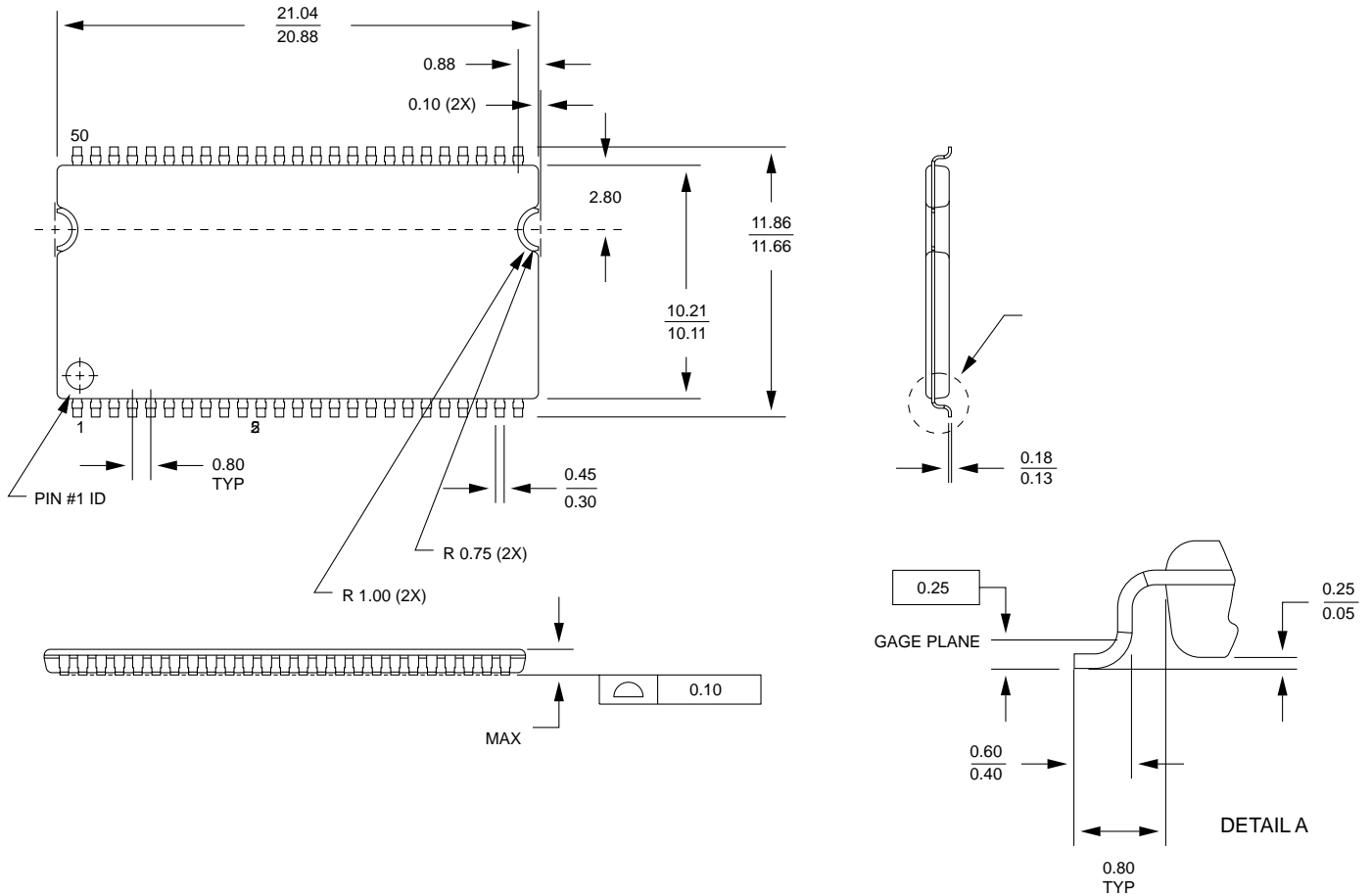
SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>AH</sub>	1		1		1		ns
t <sub>AS</sub>	2		2		2		ns
t <sub>CH</sub>	2.5		2.75		3		ns
t <sub>CL</sub>	2.5		2.75		3		ns
t <sub>CK</sub> (3)	6		7		8		ns
t <sub>CK</sub> (2)	8		10		13		ns
t <sub>CK</sub> (1)	20		25		25		ns

SYMBOL*	-7		-75		-8E		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>CKH</sub>	1		1		1		ns
t <sub>CKS</sub>	2		2		2		ns
t <sub>CMH</sub>	1		1		1		ns
t <sub>CMS</sub>	2		2		2		ns
t <sub>DH</sub>	1		1		1		ns
t <sub>DS</sub>	2		2		2		ns
t <sub>RCD</sub>	18		20		24		ns

\*CAS latency indicated in parentheses.

- NOTE:**
1. For this example, the burst length = 4.
  2. A8 and A9 = "Don't Care."
  3. DQM represents DQML and DQMH. DQML controls the lower byte, and DQMH controls the upper byte.

**50-PIN PLASTIC TSOP (400 mil)**



- NOTE:**
1. All dimensions in millimeters  $\frac{\text{MAX}}{\text{MIN}}$  or typical where noted.
  2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.01" per side.