262,144-WORD BY 16-BIT FULL CMOS STATIC RAM

DESCRIPTION

The QM55L25616B is a 4,194,304-bit static random access memory (SRAM) organized as 262,144 words by 16 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.3 to 3.3V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3mA/MHz. and a minimum cycle time of 55ns. It is automatically placed in low power mode at 0.5uA standby current (at V_{DD} = 3V, Ta = 25°C, maximum) when chip enable (CE1) is asserted high or (CE2) is asserted low. There are three control inputs. CE1 and CE2 are used to select the device and for data retention control, and output enable (OE) provides fast memory access. Data byte control pin (LB, UB) provides lower and upper byte access. This device is wellsuited to various microprocessor system applications where high speed, low power and battery backup are required.

FEATURES

- Low-power dissipation
  Operating: 9.9mW/MHz (typical)
- Single power supply voltage of 2.3 to 3.3V
- Power down features using $\overline{CE1}$ and CE2
- Data retention supply voltage of 1.5 to 3.3V
- Direct TTL compatibility for all inputs and outputs
- Standby Current (maximum):

3.3V	10 uA
3.0V	5 uA

- Access Times (maximum at V_{DD} = 2.7 to 3.3 V):

	QM55L25616B	
	5	7
Access Time	55ns	70ns
$\overline{CE1}$ Access Time	55ns	70ns
CE2 Access Time	55ns	70ns
$\overline{OE}$ Access Time	30ns	35ns

A0~A17	Address Inputs
$\overline{CE1}$, CE2	Chip Enable
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{LB}$, $\overline{UB}$	Data Byte Control
I/O1~I/O16	Data Inputs/Outputs
V_{DD}	Power
GND	Ground
NC	No Connection

Pin Assignment (Top View, 48 pin FBGA)

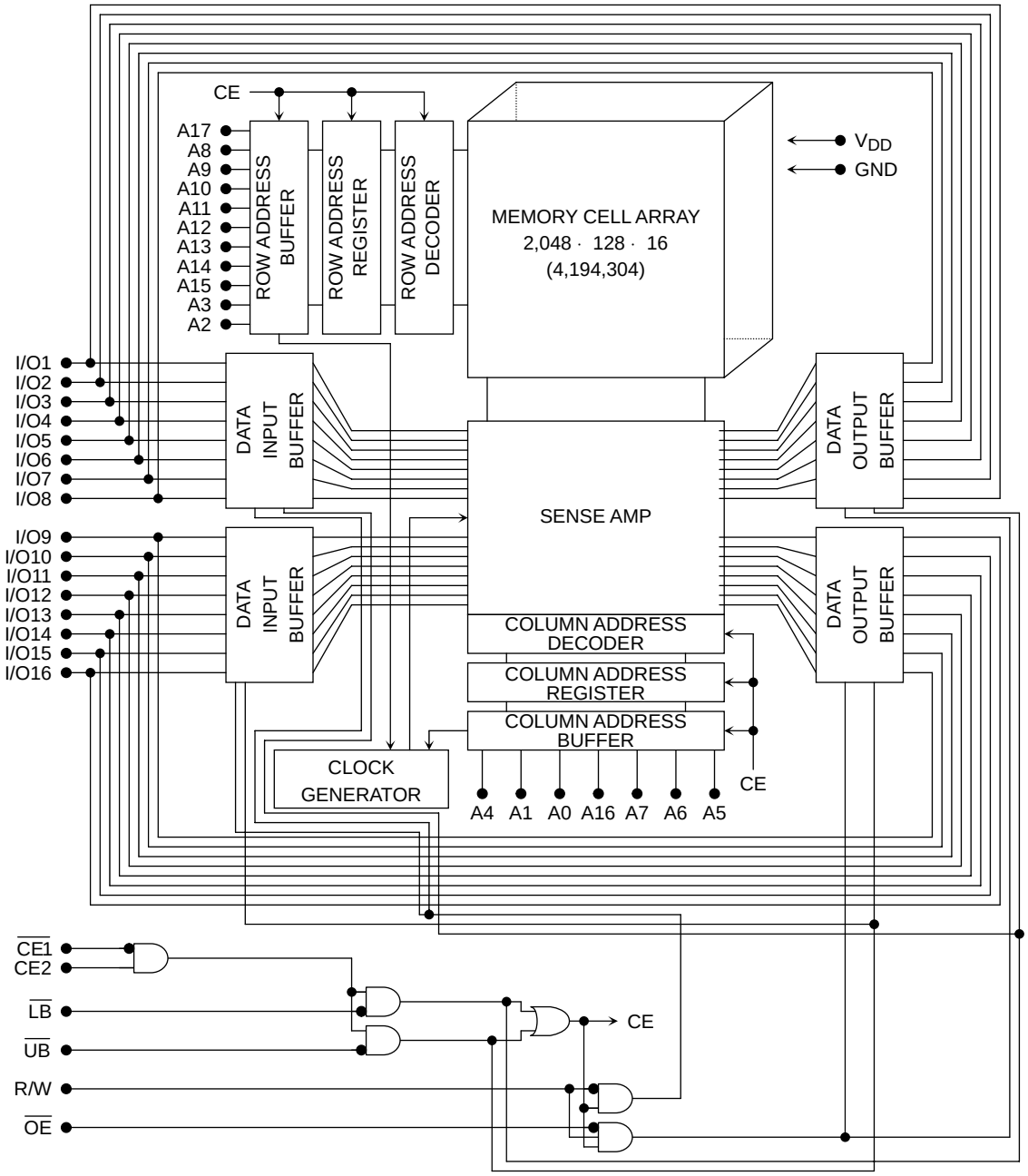
TYPE A

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	CE2
B	I/O9	$\overline{UB}$	A3	A4	$\overline{CE1}$	I/O1
C	I/O10	I/O11	A5	A6	I/O2	I/O3
D	V_{SS}	I/O12	A17	A7	I/O4	V_{DD}
E	V_{DD}	I/O13	NC	A16	I/O5	V_{SS}
F	I/O15	I/O14	A14	A15	I/O6	I/O7
G	I/O16	NC	A12	A13	R/W	I/O8
H	NC	A8	A9	A10	A11	NC

TYPE B

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	NC
B	I/O9	$\overline{UB}$	A3	A4	$\overline{CE1}$	I/O1
C	I/O10	I/O11	A5	A6	I/O2	I/O3
D	V_{SS}	I/O12	A17	A7	I/O4	V_{DD}
E	V_{DD}	I/O13	NC	A16	I/O5	V_{SS}
F	I/O15	I/O14	A14	A15	I/O6	I/O7
G	I/O16	NC	A12	A13	R/W	I/O8
H	NC	A8	A9	A10	A11	NC

BLOCK DIAGRAM



OPERATING MODE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{LB}$	$\overline{UB}$	I/O1 to 8	I/O9 to 16	Power
Read	L	H	L	H	L	L	D_{OUT}	D_{OUT}	I_{DDO}
	L	H	L	H	H	L	High-Z	D_{OUT}	I_{DDO}
	L	H	L	H	L	H	D_{OUT}	High-Z	I_{DDO}
Write	L	H	*	L	L	L	D_{IN}	D_{IN}	I_{DDO}
	L	H	*	L	H	L	High-Z	D_{IN}	I_{DDO}
	L	H	*	L	H	H	D_{IN}	High-Z	I_{DDO}
Output Deselect	L	H	H	H	*	*	High-Z	High-Z	I_{DDO}
Standby	H	*	*	*	*	*	High-Z	High-Z	I_{DDS}
	*	L	*	*	*	*	High-Z	High-Z	I_{DDS}
	*	*	*	*	H	H	High-Z	High-Z	I_{DDS}

* = don't care
H = logic high
L = logic low

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	-3.0 to 4.2	V
V_{IN}	Input Voltage	-3.0* to 4.2	V
$V_{I/O}$	Input/Output Voltage	-0.5 to V_{DD} + 0.5	V
P_D	Power Dissipation	0.6	W
T_{solder}	Soldering Temperature (10s)	260	^0C
T_{stg}	Storage Temperature	-55 to 125	^0C
T_{opr}	Operating Temperature	-40 to 85	^0C

* -2.0 V when measured at a pulse width of 20 ns

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.3	-	3.3	V
Data Retention Supply Volage	V_{DH}	1.5	-	3.3	V
Input high voltage V_{DD} = 2.3 to 3.3V	V_{IH}	2.0	-	V_{DD} +0.3	V
Input high voltage V_{DD} = 2.7 to 3.3V	V_{IH}	2.2	-	V_{DD} +0.3	V
Input low voltage	V_{IL}	-0.3*	-	V_{DD} x0.22	V

*) -2.0 V when measured at pluse width of 20ns

CAPACITANCE (Ta = 25℃, f = 1 MHz)

PARAMETER	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN} = GND	-	10	pF
Input/Output capacitance	C_{OUT}	V_{IN} = GND	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

PARAMETER	Symbol	Test Conditions			Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = 0 V to V_{DD}			-	-	±1	uA
Outout High Current	I_{OH}	V_{OH} = V_{DD} -0.5 V			-0.5	-	-	mA
Outout High Current	I_{OL}	V_{OL} = 0.4 V			2.1	-	-	mA
Output Leakage Current	I_{LO}	CE1 = V_{IH} or CE2 = V_{IL} or LB and UB = V_{IH} or R/W = V_{IL} or OE = V_{IH}, V_{OUT} = 0 V~V_{DD}			-	-	±10	uA
Operating Current	I_{DDO1}	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH} and $\overline{LB}$ and $\overline{UB}$ = V_{IL} and R/W = V_{IH} and I_{OUT} = 0 mA and Other Input = V_{IH}/V_{IL}	Tcycle	Min	-	-	45	mA
				1 us	-	-	10	
	I_{DDO2}	$\overline{CE1}$ = 0.2 V and CE2 = V_{DD} -0.2 V and $\overline{LB}$ and $\overline{UB}$ = 0.2 V, R/W = V_{DD} - 0.2 V and I_{OUT} = 0 mA, Other Input = V_{DD} - 0.2 V/0.2 V		Min	-	-	45	
				1 us	-	-	10	
Standby Current	I_{DDS1}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{LB}$ and $\overline{UB}$ = V_{IH}			-	-	2	mA
	I_{DDS2}	$\overline{CE1}$ = V_{DD} - 0.2 V or CE2 = 0.2 V or $\overline{LB}$ and $\overline{UB}$ = V_{DD} - 0.2 V, V_{DD} = 1.5 V~3.3 V	V_{DD} = 3.0 V ± 10%	Ta = 25℃	-	-	1	uA
				Ta = –40~85℃	-	-	10	
			V_{DD} = 3.0 V	Ta = 25℃	-	0.05	0.5	
				Ta = –40~40℃	-	-	1	
				Ta = –40~85℃	-	-	5	

*) In standby mode with $\overline{CE1} \geq V_{DD}$ - 0.2V, these limits are assured for the condition CE2 $\geq$ V_{DD} - 0.2V or CE2 $\leq$ 0.2V.

In standby mode with $\overline{LB}$ and $\overline{UB} \geq V_{DD}$ -0.2V, these limits are assured for the condition $\overline{CE1} \geq V_{DD}$ -0.2V or $\overline{CE1} \leq$ 0.2V and CE2 $\geq V_{DD}$ -0.2V or CE2 $\leq$ 0.2V.

AC Characteristics and Operating Condition(Ta=-40°to 85°C, V_{DD}=2.7 to 3.3V)

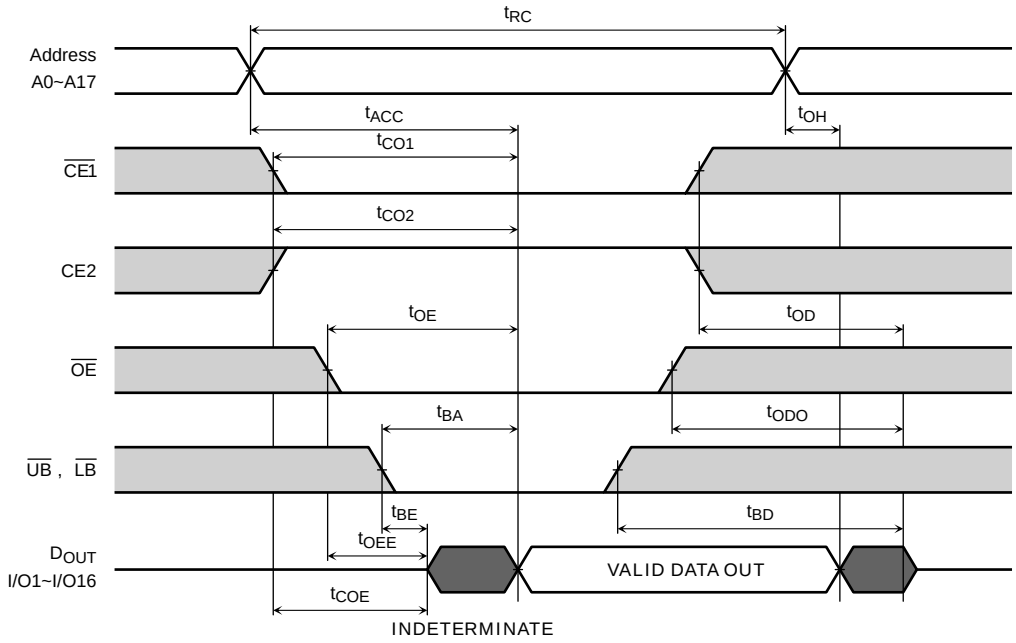
Parameter List		Symbol	Speed Bins				Units
			50ns		70ns		
			Min	Max	Min	Max	
Read	Read Cycle Time	t_{RC}	55	-	70	-	ns
	Address Access Time	t_{ACC}	-	55	-	70	ns
	Chip Enable $\overline{CE1}$ Access Time	t_{CO1}	-	55	-	70	ns
	Chip Enable CE2 Access Time	t_{CO2}	-	55	-	70	ns
	Output Enable Access Time	t_{OE}	-	30	-	35	ns
	Data Byte Control Access Time	t_{BA}	-	55	-	70	ns
	Chip Enable Low to Output Active	t_{COE}	5	-	5	-	ns
	Output Enable Low to Output Active	t_{OEE}	0	-	0	-	ns
	Data Byte Control Low to Output Active	t_{BE}	0	-	0	-	ns
	Chip Enable High to Output High-Z	t_{OD}	-	25	-	30	ns
	Outout Enable High to Output High-Z	t_{ODO}	-	25	-	30	ns
	Data Byte Control High to Output High-Z	t_{BD}	-	25	-	30	ns
	Output Data Hold Time	t_{OH}	10	-	10	-	ns
Write	Write Cycle Time	t_{WC}	50	-	70	-	ns
	Write Pulse Width	t_{WP}	45	-	50	-	ns
	Chip Enable to End of Write	t_{CW}	50	-	60	-	ns
	Data Byte Control to End of Write	t_{BW}	50	-	60	-	ns
	Address Setup Time	t_{AS}	0	-	0	-	ns
	Write Recovery Time	t_{WR}	0	-	0	-	ns
	R/W Low to Output High-Z	t_{ODW}	-	20	-	25	ns
	R/W High to Output Active	t_{OEW}	0	-	0	-	ns
	Data Setup Time	t_{DS}	25	-	30	-	ns
	Data Hold Time	t_{DH}	0	-	0	-	ns

AC Test Conditions

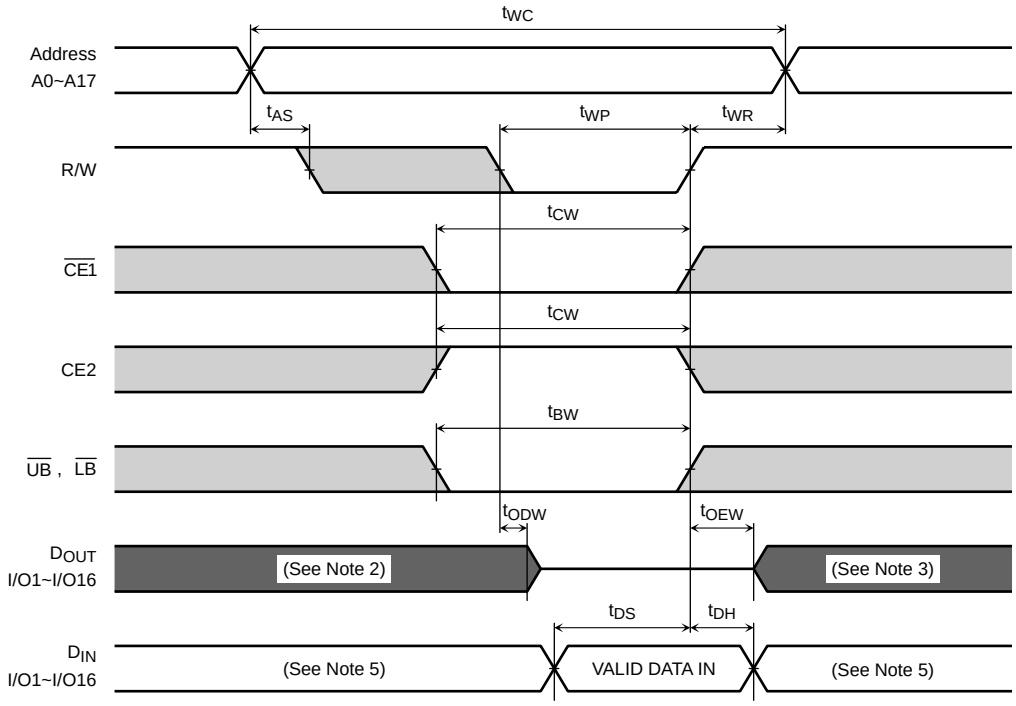
Outout load: 30 pF + 1TTL Gate
Input pulse level: 0.4V, 2.4V
Timing measuremwnts: V_{DD}x0.5
Reference level: V_{DD}x0.5
t_R, t_F: 5ns

TIMING DIAGRAMS

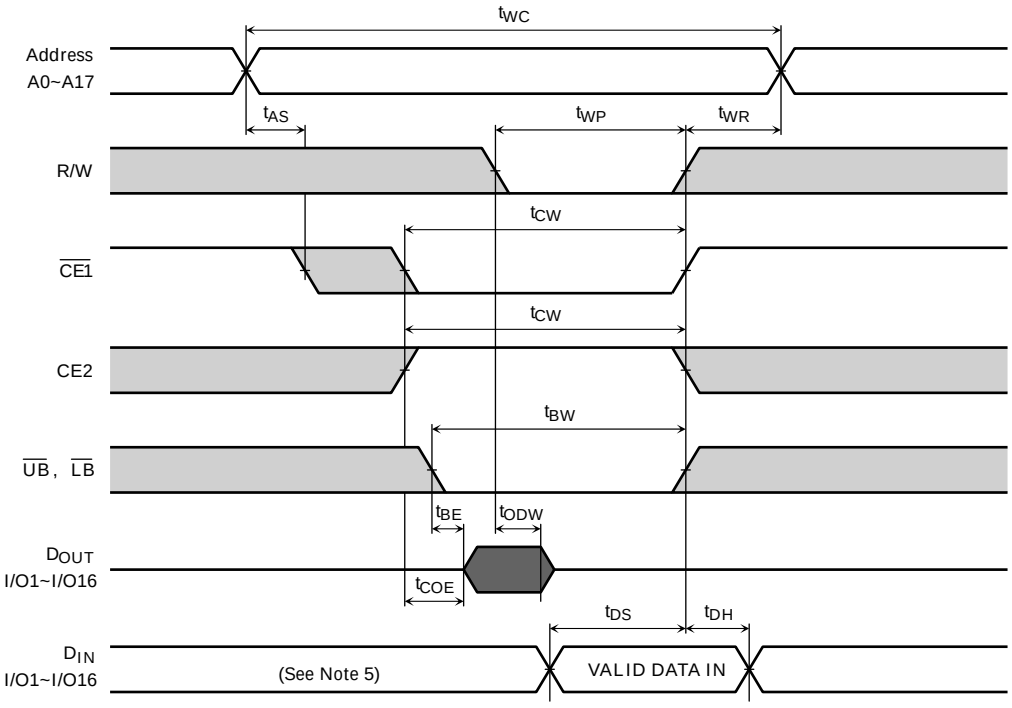
READ CYCLE (See Note 1)



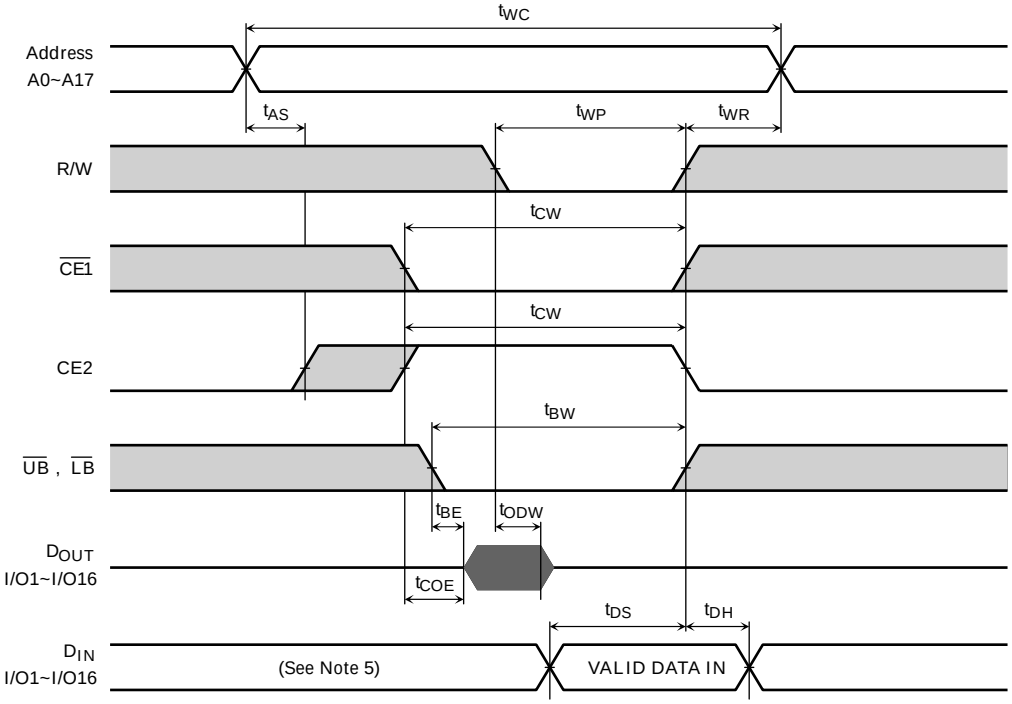
WRITE CYCLE 1 (R/W CONTROLLED)(See Note 4)



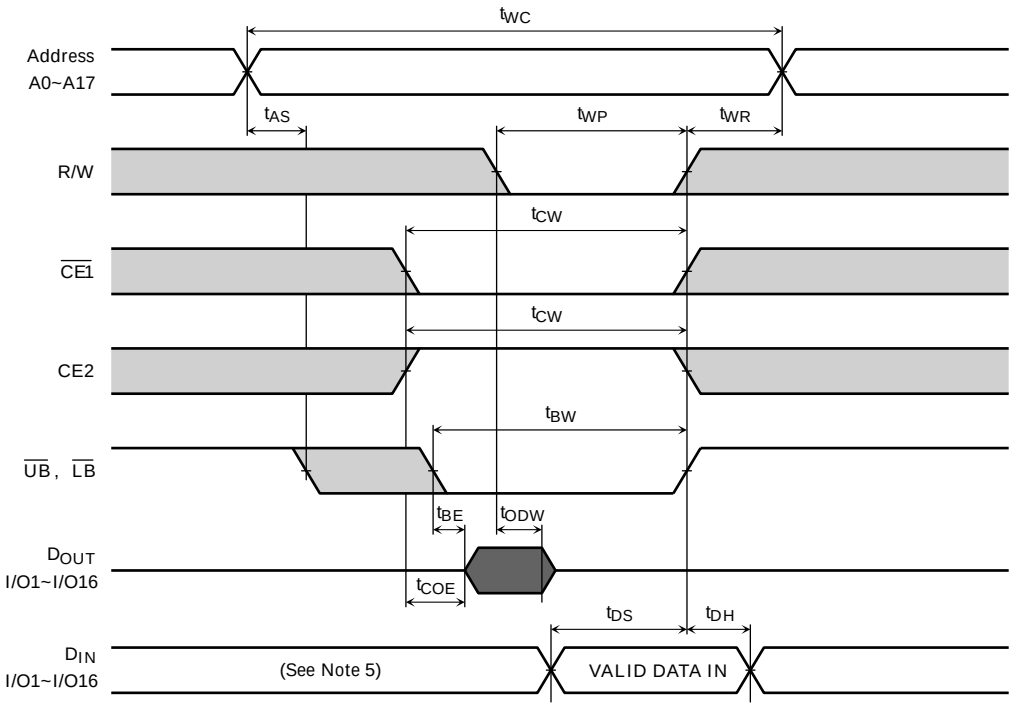
WRITE CYCLE 2 ($\overline{CE1}$ CONTROLLED) (See Note 4)



WRITE CYCLE 3 (CE2 CONTROLLED) (See Note 4)



WRITE CYCLE 4 ($\overline{UB}$, $\overline{LB}$ CONTROLLED)(See Note 4)



(1) R/W remains HIGH for the read cycle.

(2) If $\overline{CE1}$ goes LOW(or CE2 goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.

(3) If $\overline{CE1}$ goes HIGH(or CE2 goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.

(4) If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

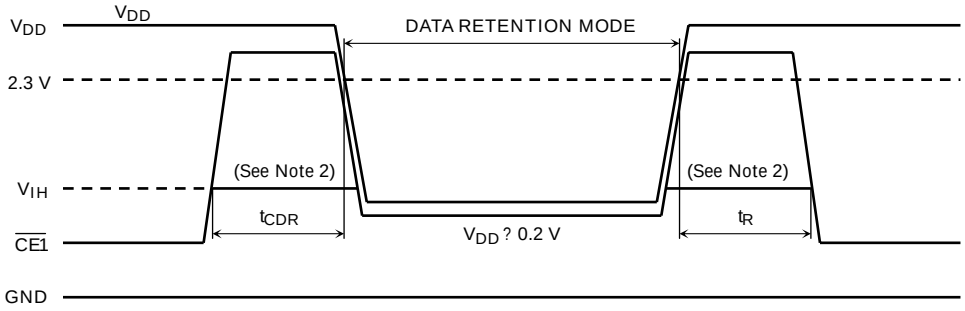
(5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS

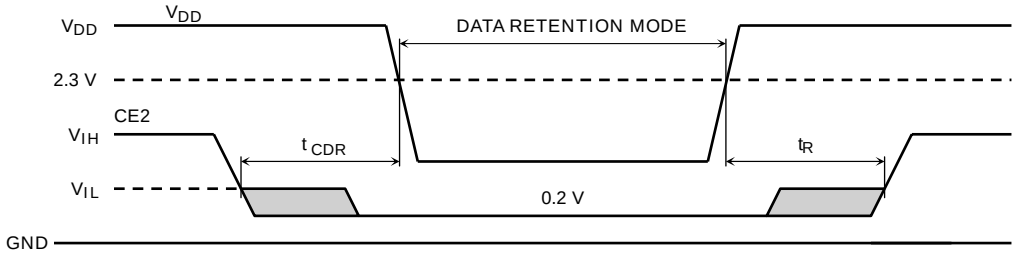
SYMBOL	PARAMETER			MIN	TYP	MAX	UNIT
V_{DH}	Data Retention Supply Voltage			1.5	-	3.3	V
I_{DDS2}	Standby Current	V_{DH} = 3.3 V	Ta = - 40~85°C	-	-	10	µA
		V_{DH} = 3.0 V	Ta = - 40~40°C	-	-	1	
			Ta = - 40~85°C	-	-	5	
t_{CDR}	Chip Deselect to Data Retention Mode Time			0	-	-	ns
t_R	Recovery Time			t_{RC} (See Note)	-	-	ns

Note: Read cycle time

$\overline{CE1}$ CONTROLLED DATA RETENTION MODE (See Note 1)



CE2 CONTROLLED DATA RETENTION MODE (See Note 3)



(1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is entered when CE2 ≤ 0.2 V or CE2 ≥ V_{DD} -0.2V

(2) When $\overline{CE1}$ is operating at the V_{IH} level, the operating current is given by I_{DDS1} during the transition of V_{DD} from 2.3 to 2.2V.

(3) In CE2 controlled data retention mode, minimum standby current mode is entered when CE2 ≤ 0.2 V.

PACKAGE OUTLINE